The constructed critical data path

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Since the completion detector detects only the constructed critical data path, the noncritical data paths do not have to transfer encoded handshake signal anymore. The logic overhead in the noncritical data paths can be reduced using single-rail domino gates instead of dual-rail domino gates. However, single-rail domino gate and dual-rail domino gate use different encoding schemes. It has encoding compatibility problem when a single-rail domino gate connects to a dual-rail domino gate. Encoding converter needs to be designed to solve the problem. In evaluation phase pc = 1, if the input is a single-rail data0 in = 0, the converter keeps the dual-rail data0. If the input is a single-rail data1 in = 1, the converter outputs a dual-rail data1 (out, out) = (1, 0). Since single-rail encoding only has two states that, respectively, represent data0 and data1, there is no other state that can be converted to spacer (out, out) = (0, 0). The disappearance of spacer violates the four-phase dual-rail protocol, which would cause data transfer error.

In practice, the robustness of the constructed critical path is affected by delay variations. As a matter of fact, it is a common problem in VLSI circuit design, same as the robustness of a clock signal in synchronous design and a match delay line in bundled-data asynchronous design. As we all know, these designs all suffer from delay variations. To resist the influence of delay variations, synchronous design enlarges the cycle time of a clock signal to get some margin. On the other hand, bundled-data asynchronous design adds extra delay margin on the matching delay line to match the worst case delay in combinational logic block. Same like these solutions, the delay variations problem in the proposed design can be solved by enlarging delay

margin on the constructed critical data path. We supply four measures to enlarge the delay margin, which are listed as follows:

1. Sizing the pull-down transistors or the static inverters of DRGs and SLGLs to increase gate delays;
2. Applying a low priority in circuit layout for the constructed critical path;
3. Improving the noncritical paths delay;
4. Adding delay elements on the critical path.

These measures have different impacts on the performance of circuits. It is better to choose a proper measure or multiple measures according to the practical design requirements. In measure:

1. Reducing the transistor size of pull-down network or the static inverters can increase the gate delays of DRGs and SLGLs. The increased delay slightly slows down pipeline speed, but smaller transistor size helps in saving power and silicon area.
2. Is layout optimization. Although this measure slightly decreases pipeline speed, it does not impose the extra overhead of transistors.
3. Does not degrade pipeline speed. The problem is that improving the noncritical path delay would increase the power consumption.
4. Is an intuitive way to enhance the critical data path. The drawback is the extra overhead of transistors.