

Intelligent campus using rfid

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chapter 1 introduction 1. 1 GENERAL With the increasing denial of time and space the RFID technology is gaining momentum day by day. RFID is a source of identification of individuals and unique products. The budding technology RFID proves to threaten even the cloning technique, through the chip insertion. New ways of improving the existing RFID technology are being found and implemented. This advancement of RFID technology is looked beyond the security purposes. 1. 2 PRESENT SCENARIO

Radio frequency identification (RFID) is a general term that is used to describe a system that transmits the identity (in the form of unique serial number) of an object wirelessly, using radio waves. RFID technologies are grouped under the more generic Automatic Identification and Data Capture (AIDC). The RFID technology is used only in security, tagging goods, inventory purposes. Since the RFID technology is not well established in India, the introduction of new methodology in the field of RFID will indeed enhance the use of RFID technology in various areas of science and technology. . 3 PROBLEM An individual should be allocated to maintain registers in all places and appointment of staffs for coordinating with students in all occasions. The ID card can be duplicated even though it has some other advancement which will be used in rare occasions. 1. 4

SOLUTION The best solution to the above problem is to develop a single RFID tag that can be used inside the college campus. Each and every RFID tag holds a particular number and it is integrated with the id cards of each and every individuals.

The RFID tag reader can be fixed anywhere in campus and it is used to collect the information about the tag location. The collected data can be sent

to centralized server to handle that information. Another added advantage is that the ID cards can't be duplicated. This has several advantages and it is a time saving one for the institution, students and staff members.

1. 5
HARDWARE AND SOFTWARE REQUIRED The hardware required is: 1) Personal computer. 2) RS 232. 3) Reader. 4) Power supply unit. 5) IR transmitter and receiver pair. 6) Buzzer. 7) LCD. 8) Tags.

The software required is: 1) AVR studio 3. 5. 2) Visual studio 6. 0. 1. 6

BLOCK DIAGRAM Figure 1. 1 block diagram of intelligent campus using RFID

CHAPTER 2 RFID system 2. 1 **INTRODUCTION** Radio Frequency Identification or RFID refers to the set of technologies that use radio waves for identifying objects or people. The RFID system is used to identify individual objects or things in the environment which can be monitored through use of wireless technology. RFID is a generic term for technologies that use radio waves to remotely store and retrieve data.

In other words, it is a combined term with RF and ID where RF means a wireless communication technology and ID means identification information of tag. So it is said that RFID is theoretically a wireless networking technology to transmit identification information stored at an electronic memory space.

2. 2 **COMPONENTS OF RFID SYSTEM:** ? An RFID device (transponder or tag), that contains data about an item. ? An antenna used to transmit the RF signals between the reader and the RFID devices. ? An RF transceiver that generates the RF signals. A reader that receives RF transmissions from an RFID device and passes the data to the host system for processing. Figure 2.

1: **RFID SYSTEM** 2. 3 **GENERIC RFID TAG ARCHITECTURE** The tag contains circuit to both rectify DC power from the incoming RF signal as well as to

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detect and extract the information modulated on the signal. The antenna load is a controlled resistance that changes the impedance of the dipole, enabling the backscatter. The tag IC is mounted on a carrier known as a strap and subsequently bonded to the antenna to form the fully assembled tag.

The chip itself is very small, enabled by modern CMOS technology. The mounting of the die on a carrier has been made very inexpensive and capable of large volume by either flip-flop or by other innovative technique such as the Alien Technologies Fluidic self Assembly process. [pic] Figure 2. 2: Basic Tag IC Architecture 2. 4 Components of a tag The major components of the tag are 1) Microchip. 2) Antenna. 2. 4. 1 Microchip Microchip is electronic equipment consisting of a small crystal of silicon semiconductor fabricated to carry out a number of electronic functions in an integrated circuit.

The microchip used in a HF tag is a contact less read/ write passive RFID device that is optimized for 13. 56 MHz RF carrier signal. The device needs an external LC resonant circuit for wireless communication with the interrogator. The device is powered remotely by rectifying an RF signal that is transmitted from the interrogator and transmits or updates its contents from memory-based on commands from interrogator. 2. 4. 2 Antenna The antenna emits the radio signal to activate the tag and reading and writing data to it.

Antennas are the conduits between the tag and the transceiver, which controls the system data acquisition and communication. Antennas are

available in a variety of shapes and sizes; they can be built in a door frame to receive tag data from persons or things. The electromagnetic field produced by an antenna can be constantly present when multiple tags are expected continuously. If constant interrogation is not required, the field can be activated by the sensor device. 2. 5 rfid readers RFID reader is like any other device that can be connected to a PC Or might be in built like an external or internal modem.

The RFID reader can be powered by a power source using an adapter "Reader" or "Interrogator", a device that is able to locate and activate tags so that the information that has been programmed onto the tag is transmitted back to the reader and subsequently to interface computing systems. The information that is received by the reader is then passed to the backend computing system to initiate the events, transactions, workflows, etc. Not only do reader locate activate and receive transmissions from RFID tags, a reader has the ability of sending data back to read/write capable tag in order to append or replace data.

Readers exist that can also scan bar codes in environments where both bar codes and RFID are used. 2. 6 COMPONENTS OF A READER The reader has the following main components: ? Transmitter and Receiver ? Microprocessor ? Memory ? I/O channels for external sensors, actuators and annunciators ? Controller ? Communication interface ? Power. [pic] Figure 2. 3: BLOCK diagram of a reader 2. 6. 1 TRANSMITTER The reader's transmitter is used to transmit AC power and the clock cycle via antennas to the tags in its read zone.

This is part of the transceiver unit, the component responsible for sending the reader signal to the surrounding environment and receiving tag responses back via the reader antennas. The antenna ports of reader are connecting to its transceiver component. One reader antenna can be attached to each such antenna port. Receiver receives analog signals from the tag via the reader antenna. It then sends the signals to reader microprocessor, where it is converted to its equivalent digital form.

2. 6. 2 MICROPROCESSOR

This component is responsible for implementing the reader protocol to communicate with compatible tags.

It performs decoding and error checking of the analog signal from the receiver. In addition, the microprocessor might contain custom logic for doing low level filtering and processing of read tag data.

2. 6. 3 MEMORY

Memory is used for storing data such as the reader configuration parameters and list of tag reads. Depending on the memory size, however, a limit applies as to how many such tag reads can be stored at one time. If the connection remains down for an extended period with the reader reading tags during this downtime, this limit might be exceeded and part of the stored data lost.

2. 6. 4 I/O channels

Readers do not have to be turned on for reading tags at all time. A sensor of some sort, such as a motion or light sensor, detects the presence of tagged objects in the readers read zone. This sensor can then set the reader on to read this tag. Similarly, this component also allows the reader to provide local output depending on some condition via an annunciators or an actuator.

2. 6. 6 CONTROLLER

A controller is an entity that allows an external entity, either a human or a computer program, to communicate with and

control a reader's function and to control annunciators and actuators associated with the reader. . 6. 7 COMMUNICATION INTERFACE The communication interface component provides the communication instructions to a reader that allows it to interact with external entities, via a controller to transfers its stored data and to accept commands and send back the corresponding responses. 2. 6. 8 POWER This component supplies power to the reader component. The power sources generally provided to this component through a power cord connected to an appropriate external electrical outlet. 2. 7 COMMUNICATION BETWEEN A READER AND A TAG

Depending on the tag type, the communication between the reader and a tag can be one of the following:

- Modulated backscatter
- Transmitter type
- Transponder type

The area between a reader antenna and one full wave length of the RF wave emitted by the antenna is called near field. The area beyond one full wavelength of the RF wave emitted from a reader antenna is called far field. Passive rfid systems operating in LF and HF use near field communication, whereas those in UHF and microwave frequencies use far field communication.

The signal strength in near field communication attenuates as the cube of the distance from the reader antenna. In far field, it attenuates as square of the distance from the reader antenna. 2. 7. 1 MODULATED BACK SCATTER Modulated backscatter communication applies to passive as well as to semi active tags. In This type of communication, the reader sends out a continuous wave (CW) RF signal containing ac power and clock signal to the tag at carrier frequency. Through physical coupling, the antennas supplies

power to the microchip. About 1.2V are generally necessary to energize the tag microchip for reading microchips.

For writing, the microchip usually needs to draw about 2.2V from the reader signal. The microchip now modulates or breaks up the input signal into a sequence of on and off patterns that represents its data and transmits it back. When the reader receives this modulated signal, it decodes the pattern and obtains the data. Thus, in modulated backscatter communication, the reader always “talks” first, followed by the tag. A tag using this scheme cannot communicate at all in the absence of a reader because it depends totally on the reader’s power to transmit its data. [pic] Figure 2.4:

backscatter communication 2.7.2 TRANSMITTER TYPE This type of communication applies to active tags only. In this type of communication, the tag broadcasts its message to the environment in regular intervals irrespective of the presence or absence of a reader. Therefore, in this type of communication, the tag always “talks” first rather than the reader. [pic]

Figure 2.5: TRANSMITTER communication 3.4.3 TRANSPONDER TYPE In this type of communication, the tag goes to a “sleep” or into a dormant stage in the absence of interrogation from a reader.

In this stage, the tag might periodically send a message to check any reader is listening to it. When a reader receives such a query message, it can instruct the tag to “wake up” or end the dormant stage. When the tag receives this command from the reader, it exits its current state and starts to act as a transmitter tag again. The tag data is sent only the reader specially asks. [pic] Figure 2.6: TRANSPONDER communication chapter 3

microcontroller 3.1 INTRODUCTION The hardware includes the following

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components: ? Atmega162 (micro controller). ? Power supply. ? In system programming. ? Buzzer. Liquid crystal display. ? Reset. ? Max 232. 3. 2

Hardware details of ATMEGA162 controller Utilizes the AVR – RISC architecture. 3. 2. 1 Features ? High-performance and Low-power Advanced RISC Architecture. ? Most single clock execution. ? 32 x 8 general purpose working registers. ? Fully static operation. ? On chip 2 cycle multiplier. ? Up to 16 MIPS throughput at 16 MHz. ? 131 powerful instructions. 3. 2. 2 Non-volatile Program and Data Memories? 16K Bytes of In-System Self-programmable Flash. ? Endurance: 10, 000 Write/Erase Cycles. ? 512 Bytes EEPROM. ? 1K Bytes Internal SRAM. Up to 64K Bytes Optional External Memory Space. ? Programming Lock for Flash program and EEPROM data Security. 3. 2. 3 Peripheral Features ? Two 8-bit Timer/Counters with Separate Modes. ? Two 16-bit Timer/Counters with Separate Compare Modes, and Capture Modes. ? Real Time Counter with Separate Oscillator. ? Six PWM Channels. ? Dual Programmable Serial USARTs. ? Master/Slave SPI Serial Interface. ? Programmable Watchdog Timer with Separate On-chip Oscillator. ? On-chip Analog Comparator. ? External and internal interrupt sources. 3. 2. 4 SPECIFICATION ? Low power high speed CMOS process technology. Fully static operation. ? Power consumption at 4 MHz, 3v, 25c. ? Active: 3. 0 MA. 3. 2. 5 Special Microcontroller Features ? Power-on Reset and Programmable Brown-out Detection. ? Internal Calibrated RC Oscillator. ? External and Internal Interrupt Sources. ? Five Sleep Modes: Idle, Power-save, Power-down, Standby, and Extended Standby. 3. 2. 6 I/O and Packages ? 35 Programmable I/O Lines. ? 40-pin PDIP, 44-lead TQFP, and 44-pad MLF. 3. 2. 7 Operating Voltages ? 1. 8 - 5. 5V for ATmega162V. ? 2. 7 - 5. 5V for ATmega162. 3. 2. 8 Speed Grades ? 0 - 8 MHz for ATmega162V. ? 0 - 16 MHz

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for ATmega162. 3. ATMEGA162 architectural overview The ATmega162 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega162 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed. The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. . 3. 1 features OF ATMEGA162 The 16K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 1K bytes SRAM, an external memory interface, 35 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, four flexible Timer/Counters with compare modes, internal and external interrupts, two serial programmable USARTs, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File - in one clock cycle. Six of the 32 registers can be used as three 16-bit indirect addresses register pointers for Data Space addressing - enabling efficient address calculations. One of

these address pointers can also be used as an address pointer for look up tables in Flash Program memory.

These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section. The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation. [pic] Figure 3. 1: BLOCK Diagram. Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space.

Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16 or 32-bit instruction. [pic] Figure 3. 2: BLOCK Diagram of the AVR Architecture Program Flash memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section. During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack.

The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). [pic] Figure 3. 3: Data Memory Map

3. 3. 2 ALU – Arithmetic Logic Unit The high-performance AVR ALU operates in direct connection with all the 32 general purpose

working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions.

3.3.3 Status Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations.

Status Register format [pic]

Bit 7 – I: Global Interrupt Enable: The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers.

If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts.

Bit 6 – T: Bit Copy Storage: The Bit Copy instructions BLD (Bit Load) and BST (Bit Store) use the T bit as source or destination for the operated bit.

Bit 5 – H: Half Carry Flag: The Half Carry Flag H indicates a half carry in some arithmetic operations.

Half Carry is useful in BCD arithmetic.

Bit 4 – S: Sign Bit, S = N. V: The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V.

Bit 3 – V: Two's Complement Overflow Flag: The Two's Complement Overflow Flag V supports two's complement arithmetic.

Bit 2 – N: Negative Flag: The Negative Flag N indicates a negative result in an arithmetic or logic operation.

Bit 1 – Z: Zero Flag: The Zero Flag Z

indicates a zero result in an arithmetic or logic operation. Bit 0 – C: Carry Flag:

The Carry Flag C indicates a carry in an arithmetic or logic operation. 3. 3. 4 Stack Pointer The Stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The Stack Pointer Register always points to the top of the Stack. The Stack Pointer points to the data SRAM Stack area where the Subroutine and Interrupt Stacks are located. This Stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. Stack Pointer FORMAT pic] The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt RETI. The AVR Stack Pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. 3. 3. 5 Reset and Interrupt Handling The AVR provides several different interrupt sources. These interrupts and the separate Reset Vector each have a separate program vector in the program memory space.

All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. There are basically two types of interrupts. The first type is triggered by an event that sets the Interrupt Flag. For these interrupts, the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, and hardware clears the

corresponding Interrupt Flag. Interrupt Flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

If an interrupt condition occurs while the corresponding interrupt enable bit is cleared, the Interrupt Flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software. The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have Interrupt Flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

3. 3. 6 In-System Reprogrammable Flash Program Memory

The ATmega162 contains 16K bytes On-chip In-System Reprogrammable Flash memory for program storage.

Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 8K x 16. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section. [pic]

Figure 3. 4 Programmable Memory Map The Flash memory has an endurance of at least 10, 000 write/erase cycles. The ATmega162 Program Counter (PC) is 13 bits wide, thus addressing the 8K program memory locations.

3. 4 EEPROM Data Memory

The ATmega162 contains 512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written.

The EEPROM has an endurance of at least 100, 000 write/erase cycles. The access between the EEPROM and the CPU is described in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and the EEPROM Control Register.

3. 4. 1 EEPROM Read/Write Access

The

EEPROM Access Registers are accessible in the I/O space. A self timing function, however, lets the user software detect when the next byte can be written. If the user code contains instructions that write the EEPROM, some precautions must be taken. In heavily filtered power supplies, VCC is likely to rise or fall slowly on Power-up/down.

This causes the device for some period of time to run at a voltage lower than specified as minimum for the clock frequency used. In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. The EEPROM Address Register [pic] Bits 15. 9 – Res: Reserved Bits These bits are reserved bits in the ATmega162 and will always read as zero. Bits 8. 0 – EEAR8. 0: EEPROM Address The EEPROM Address Registers – EEARH and EEARL specify the EEPROM address in the 512 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 511. The initial value of EEAR is undefined.

A proper value must be written before the EEPROM may be accessed. The EEPROM Data Register – EEDR [pic] Bits 7. 0 – EEDR7. 0: EEPROM Data For the EEPROM write operation, the EEDR Register contains the data to be written to the EEPROM in the address given by the EEAR Register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR. The EEPROM Control Register – EECR [pic] Bits 7. 4 – Res: Reserved Bits These bits are reserved bits in the ATmega162 and will always read as zero. Bit 3 – EERIE: EEPROM Ready Interrupt Enable

Writing EERIE to one enables the EEPROM Ready Interrupt if the I bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready interrupt generates a constant interrupt when EEWEIF is cleared. Bit 2 – EEMWE: EEPROM Master Write Enable The EEMWE bit determines whether setting EEWEIF to one cause the EEPROM to be written. When EEMWE is set, setting EEWEIF within four clock cycles will write data to the EEPROM at the selected address. If EEMWE is zero, setting EEWEIF will have no effect. When EEMWE has been written to one by software, hardware clears the bit to zero after four clock cycles.

See the description of the EEWEIF bit for an EEPROM write procedure. Bit 1 – EEWEIF: EEPROM Write Enable The EEPROM Write Enable signal EEWEIF is the write strobe to the EEPROM. When address and data are correctly set up, the EEWEIF bit must be written to one to write the value into the EEPROM. The EEMWE bit must be written to one before a logical one is written to EEWEIF; otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 3 and 4 is not essential): 1. Wait until EEWEIF becomes zero. 2.

Wait until SPEN in SPMCR becomes zero. 3. Write new EEPROM address to EEAR (optional). 4. Write new EEPROM data to EEDR (optional). 5. Write a logical one to the EEMWE bit while writing a zero to EEWEIF in EECR. 6. Within four clock cycles after setting EEMWE, write a logical one to EEWEIF. The EEPROM can not be programmed during a CPU write to the Flash memory. The software must check that the Flash programming is completed before initiating a new EEPROM write. Step 2 is only relevant if the software contains a Boot Loader allowing the CPU to program the Flash.

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If the Flash is never being updated by the CPU, step 2 can be omitted.

Caution: An interrupt between step 5 and step 6 will make the write cycle fail, since the EEPROM Master Write Enable will time-out. If an interrupt routine accessing the EEPROM is interrupting another EEPROM access, the EEAR or EEDR Register will be modified, causing the interrupted EEPROM access to fail. It is recommended to have the Global Interrupt Flag cleared during all the steps to avoid these problems. When the write access time has elapsed, the EWE bit is cleared by hardware.

The user software can poll this bit and wait for a zero before writing the next byte. When EWE has been set, the CPU is halted for two cycles before the next instruction is executed. Bit 0 – EERE: EEPROM Read Enable The EEPROM Read Enable Signal EERE is the read strobe to the EEPROM. When the correct address is set up in the EEAR Register, the EERE bit must be written to a logic one to trigger the EEPROM read. The EEPROM read access takes one instruction, and the requested data is available immediately. When the EEPROM is read, the CPU is halted for four cycles before the next instruction is executed.

The user should poll the EWE bit before starting the read operation. If a write operation is in progress, it is neither possible to read the EEPROM, nor to change the EEAR Register. 3. 5 Timing External memory devices have various timing requirements. It is important to consider the timing specification of the external memory device before selecting the wait-state. The most important parameters are the access time for the external memory in conjunction with the set-up requirement of the ATmega162. [pic] Figure 3. 5: External Data Memory Cycles without Wait-state. 3. 6 Crystal Oscillator
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XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator. Either a quartz crystal or a ceramic resonator may be used. C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. The Oscillator can operate in four different modes, each optimized for a specific frequency range. [pic] Figure 3. 6: Crystal Oscillator Connections 3. 6. 1 Low-frequency Crystal Oscillator

The Low-frequency Crystal Oscillator must be selected by setting the CKSEL Fuses to “ 0100”, “ 0101”, “ 0110” or “ 0111”. The crystal should be connected as shown in Figure. If CKSEL equals “ 0110” or “ 0111”, the internal capacitors on XTAL1 and XTAL2 are enabled, thereby removing the need for external capacitors. The internal capacitors have a nominal value of 10 pF. When this Oscillator is selected, start-up times are determined by the SUT Fuses (real time-out from Reset) and CKSEL0 (number of clock cycles) as shown in below tables [pic] Table 4. 1 Start-up DELAYS from Reset when Low-frequency Crystal Oscillator is selected . 7 Watchdog Timer If the Watchdog Timer is not needed in the application, this module should be turned off. If the Watchdog Timer is enabled, it will be enabled in all sleep modes, and hence, always consume power. In the deeper sleep modes, this will contribute significantly to the total current consumption. Chapter 4

monitoring every individual inside the campus. 4. 2 Basic setup [pic]Figure 4. 1 basic setup

The basic external setup for the project is shown in figure 8. 1. The HF reader is connected to microcontroller through RS-232 cable and the IR pairs are connected to the port pins of microcontroller. The microcontroller is then connected to the host computer (server) through RS-232 cable. The detailed explanation of the blocks are given below 4. 3 PERIPHERALS 4. 3. 1 I/O

PORTS All AVR ports have true read-modify-write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions.

Port A Port A is an 8-bit bi-directional I/O port. Three I/O memory address locations are allocated for the Port A, one each for the Data Register – PORT A, \$3B(\$3B), Data Direction Register – DDRA, \$3A(\$3A) and the Port A Input Pins – PINA, \$39(\$39). The Port A Input Pins address is read only, while the Data Register and the Data Direction Register are read/write. Port B Port B is an 8-bit bi-directional I/O port. Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORT B, \$38(\$38), Data Direction Register - DDRB, \$37(\$37) and the Port B Input Pins – PINB, \$36(\$36).

The Port B Input Pins address is read only, while the Data Register and the Data Direction Register are read/write. Port C Port C is an 8-bit bi-directional I/O port. Three I/O memory address locations are allocated for the Port C, one each for the Data Register – PORT C, \$35(\$35), Data Direction Register –

DDRC, \$14(\$34) and the Port C Input Pins - PINC, \$13(\$33) The Port C Input Pins address is read only, while the Data Register and the Data Direction Register are read/write. Port D Port D is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port D, one each for the Data Register - PORT D, \$12(\$32), Data Direction Register - DDRD, \$11(\$31) and the Port D Input Pins - PIND, \$10(\$30). The Port D Input Pins address is read only, while the Data Register and the Data Direction Register are read/write. 4. 4 USART (Universal Synchronous and Asynchronous serial Receiver and Transmitter): The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are: ?

Asynchronous or Synchronous Operation ? Master or Slave Clocked Synchronous Operation ? Odd or Even Parity Generation and Parity Check Supported by Hardware ? Data Overrun Detection ? Framing Error Detection ? Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete ? Multi-processor Communication Mode ? Double Speed Asynchronous Communication Mode The ATmega162 has two USARTs, USART0 and USART1. USART0 and USART1 have different I/O Registers. Portd0 is the receiver pin and portd1 is the transmitter pin.

Here we are using IC MAX232 as a UART driver. [pic] Figure 4. 2 uart driver.

4. 4. 1 AVR UART - Compatibility The USART is fully compatible with the AVR UART regarding: ? Bit locations inside all USART Registers ? Baud Rate Generation ? Transmitter Operation ? Transmit Buffer Functionality ? Receiver Operation 4. 4. 2 USART Initialization The USART has to be

initialized before any communication can take place. The initialization process normally consists of setting the baud rate, setting frame format and enabling the Transmitter or the Receiver depending on the usage.

For interrupt driven USART operation, the Global Interrupt Flag should be cleared (and interrupts globally disabled) when doing the initialization. The TXC Flag can be used to check that the Transmitter has completed all transfers, and the RXC Flag can be used to check that there are no unread data in the receive buffer. 4. 5 SENSOR Sensors are the devices that are used to convert the physical parameter into signal that can be measured electrically and it can be easily given as an input to the microcontroller. The effectual sensor should have the following properties namely, ?

Sensor should be sensitive to measured property. ? It should be insensitive to any other property. ? It should not influence any other property. An IR sensor is used. It uses IR LED as an IR transmitter, which emits IR rays in the wavelength of 940 nm and a phototransistor is used as IR receiver, which detects IR rays and the output comes in collector. If the receiver is receiving IR rays the output will be low otherwise output is high. The output of the receiver is given to the comparator chip LM393, which compares the receiver output with the prefixed voltage signal.

The output of the comparator is given to microcontroller. [pic] Figure 4. 3
CIRCUIT DIAGRAM OF IR SENSOR 4. 5. 1 IR TRANSMITTER LED, a special type of semiconductor diode that has a pn junction acts as a transmitter. The wavelength and the color of the light depend on the band gap energy of the material forming pn junction. The materials used for a LED have a direct

band gap energy corresponding to near IR, but Germanium and silicon are indirect band gap materials resulting in a non – radiative recombination. Hence does not emit light. The advantages of LED over incandescent sources are: ? Less costly Long life p ? Insensitive to vibration and shocks. 4. 5. 2 IR RECEIVER A phototransistor is used to detect the IR rays from the LED. It is a bi polar junction that is encased in a transparent case so that light can reach the base collector junction. The phototransistor works like a photodiode with a very high very high sensitivity for light, because the electrons that are generated by photons in the base collector junction are injected to base and amplified like a transistor. It has a slower response time than photodiode.

[pic] Figure 4. 4 BLOCK DIAGRAM OF IR SENSOR 4. 5. 3 COMPARATOR

The comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. For an inverting comparator the reference voltage is applied to the (+) input and input is given to the (-) terminal. The common mode voltage range includes ground, and the differential input voltage equals power supply voltage. [pic]

Figure 4. 5: PIN CONFIGURATION OF LM 393 4. 6 BUZZER It is a transducer which converts electrical signal to sound signal. Piezoelectricity is the ability of certain crystals to produce a voltage when subjected to mechanical stress. The effect is reversible (i. .) crystals when subjected to external applied voltage can change shape by a small amount and the effect is of nanometers. [pic] Figure 4. 6 circuit diagram of buzzer 4. 7 RS-232C RS-232

stands for Recommend Standard number 232 and C is the latest revision of the standard. The serial ports on most computers use a subset of the RS-232C standard. [pic] Figure: 4. 7. RS-232 CONNECTOR 4. 7. 1 DB9

INFORMATION The DB9 connection has 9 pins which are each described in the below table. The illustration below is an example of the female serial connector, which would usually be located on the connector that would connect to the computer. 9 pin connector on a DTE device (PC connection) | |

Pin No	Direction of the signal	1	Carrier(CD) (from DCE) incoming signal from the modem	2	Received data (RD) incoming data from DCE	3	Transmit data (TD) outgoing data to a DCE	4	Data terminal ready (DTR) outgoing handshake signal	5	Signal ground common reference voltage	6	Data set ready (DSR) incoming handshaking signal	7	Request to send (RTS) outgoing flow control signal	8	Clear to send (CTS) incoming flow control signal	9	Ring indicator (RI) (from DCE) incoming signal from a modem
Table: 4. 1: DB9 connector DTE stands for Data Terminal Equipment, and DCE stands for Data Communications Equipment.																			

These terms are used to indicate the pin-out for the connectors on a device and the direction of the signals on the pins The RS-232 standard states that DTE devices use a 9-pin male connector, and DCE devices use a 9-pin female connector. 4. 8 LCD LCD is an output device which is used to display a character or a text through microcontroller. So, the LCD is connected in the output port pins of microcontroller. A 2 line LCD display has totally 32 pins. 32 characters can be displayed in our LCD. [pic] Figure 4. 8: 16x2 LCD

DISPLAY The starting address for the first line is \$80 and for end address is \$8F and for second line the starting address is \$C0 and the end address is \$CF. Pin no | Pin name | I/P or O/P | External connection | Function | | 1 | VSS | -- | Power supply | GND | | 2 | VDD | -- | +5V | | 3 | VO | -- | V lcd adjustment | | 4 | RS | I/p | MPU | Register select signal | | 5 | R/W | I/p | MPU | Read/write

select signal | | | | | Read-1; write-2. | | 6 | E | I/p MPU | Operation enable
 signal | | 7-10 | DB0-DB3 | I/p | MPU | Lower order lines | | 11-14 | DB4-DB7 |
 I/p | MPU | Higher order lines | | 15-16 | LED,,+,, | I/p | LED backlight power
 supply | LED,,+,, voltage | | LED,,-,, | | type : 4. 2V; Max: 4. 5V | | | | |
 LED,,-,, : GND | Table 4. 2 discription of lcd terminals Chapter 5 VISUAL BASIC

5. 1 INTRODUCTION The Visual Basic language is quite powerful – if one can imagine a programming task; it can probably be accomplished using Visual Basic.

Once the basics of Visual Basic are understood then one becomes productive. 5. 2 About Visual Basic The “ Visual” part refers to the method used to create the graphical user interface (GUI), Rather than writing numerous lines of code to describe the appearance and location of interface elements, simply add pre built objects into place on screen. The “ Basic” part refers to the BASIC (Beginners All-Purpose Symbolic Instruction Code) language, a language used by more programmers. Visual Basic has evolved from the original BASIC languages and now contains several hundred statements, functions, and keywords, many of which relate directly to the Windows GUI.

Beginners can create useful applications by learning just a few of the keywords, yet the power of the language allows professionals to accomplish anything that can be accomplished using any other Windows programming language. The Visual Basic programming language is not unique to Visual Basic. The Visual Basic programming system, Applications Edition included in Microsoft Excel, Microsoft Access, and many other Windows applications uses the same language. The Visual Basic Scripting Edition (VB Script) is a widely
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used scripting language and a subset of the Visual Basic language. The investment one makes in learning Visual Basic will carry over to many other areas.

Whether the goal is to create a small utility for an individual, a work group a large enterprise-wide system, or even distributed applications pning the globe via the Internet, Visual Basic has the required tools. 5. 3

ADVANTAGES ? Data Access features allow you to create databases, front-end applications, and scalable server-side components for most popular database formats, including Microsoft SQL Server and other enterprise-level databases. ? ActiveXTM Technologies allow you use the functionality provided by other applications, such as Microsoft Word Processor, Microsoft Excel spreadsheet, and other Windows applications.

Even applications can be automated and objects can be created using the Professional or Enterprise editions of Visual Basic. ? Internet capabilities make it easy to provide access to documents and applications across the Internet or intranet from within the application, or to create Internet server applications. ? The finished application is a true. exe file that uses a Visual Basic Virtual Machine that you can freely distribute. 5. 4 Program description

The front end is visual basic and this programming concept is chosen because it is more users friendly. The information or the status about the persons is displayed and the same can be stored in a database so that it can be accessed later. [pic] Figure 5. : output and database creation, checking

form Chapter 6 conclusion RFID technology is a budding technology that is fast growing world wide. RFID proves to be cutting edge technology through its applications. This project moves a step ahead in RFID's application and <https://assignbuster.com/intelligent-campus-using-rfid/>

presents a new dimension to view through. This project proves to be entirely different and innovative of RFID technology with the existing components. Such an introduction of a new methodology in the RFID technology enhances its use and improves the present knowledge. The project “ INTELLIGENT campus using RFID” will sure make a great difference in the present industrial applications of RFID.

It will provide the ultimate solution for the problems that exists in various cases. This is a prototype of the proposed idea wherein the entire reason behind it is to provide a fully compact, covering larger distance. 6. 1

PROCESS EXPLANATION The various processes that take place during the working of the project are as follows: The RFID tag is a passive, high frequency device in which some unique data's can be stored in the form of serial numbers known as ELECTRONIC PRODUCT CODE (EPC). Whenever the RFID tag comes in the field of a particular reader, the reader detects the tag and sends the detected information about the EPC to the microcontroller.

ACTIVITY FLOWCHART Figure 6. 1: activity flow chart

The received information will be fed into the microcontroller which compares the epc number to specific information's about group of individuals. If the received information is already in the list, it will allow the user to enter inside the campus and also maintains a database for storing this information. The reader refreshes its data continuously checks after certain amount of time interval and when the RFID reader detects the absence of a tag it will remove the tag details from the list. The database can be created with the help of visual basic programming. [pic] Figure 6. 2: database creation of persons entering into the campus Whenever the tag enters into a specific

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location such as class rooms, library etc, the reader present in that location will detects the tag.

Two IR transmitter - receiver pairs are used for the purpose of monitoring whether the person is entering the room or leaving the room. The IR rays interfering sequence is fed to the microcontroller and it is used for detecting the status of the person having that particular tag. The details or the status are also saved into database using visual basic coding. The databases can be shared in the network and it can be used for finding or monitoring each and every individual belonging to that campus. [pic] Figure 6. 3: database creation of persons entering into PARTICULAR LOCATION. The same can be used to find the individual location using search option. 6. 2 FUTURE ENHANCEMENTS

The project could further be developed and enhanced in an effective way by suitable polarization RFID reader antennas and increasing the frequency range so that it would not only provide the solution for monitoring persons in a smaller area as mentioned in this model. The security can also be increased by replacing IR devices by some bio-metric ideas. -----

162- MICRO CONTROLLER LCD I/O P O R T S I/O P O R T S BUZZER IR 1 IR 2
 USART USART PC RFID END CREATES A DATA BASE (In/Out) 1-2 OR 2-1 Yes
 No Interruption Occurred CHECHS FOR IR SIGNAL CREATES A DATA BASE
 (Present inside the campus) INFORMATION TRANSFER FROM RFID READER
 TO M162 Yes RFID TAG PRESENT No READER SIGNAL TRANSMIT START