Final exam summary assignment

Your sheet must not be typed (even part of it) and oh can’t photocopy someone else’s shell You can also bring a calculator. NO cell phones, not even as time-pieces. In terms of material, the final will cover everything up to the end of Slide Set 14 (not Slide Set 15). More specifically, we have covered this (this is not a complete list): Slide Set 1: Introduction: not a lot to study here Slide Set 2: Combinational Logic: In this section, we talked about combinational logic, and how to specify combinational logic in PHD We talked about structural specifications, packages, libraries, buses, attributes of buses, and stud_logic vs.. It. In previous years, we talked about the ‘ With” and “ when” statement, however I didn’t discuss that this year, because they are not that commonly used, Slide Set 3: The process and Sequential Circuits: In this section, we thirst talked about how to implement a OFF using a process We then generalized it a bit to talk about state machines, We also talked about asynchronous vs.. Synchronous resets. Then we talked about how to implement combinational logic using a process.

Slide Set 4: In Slide Set 4, the focus was on how to write Synthesize PHD. Remember, the underlying rule is that each recess in your design has to fall into one of the three categories I described: purely combinational, purely sequential, and sequential with an asynchronous set and reset. Surely, on the exam, you will be asked to verity “ synthesize PHD”, and you’ll lose marks four code is not synthesize. Just remember to follow the rules in this Slide Set, and you Will be fine.

Slide Set S: In this slide set, we talked some more about the Process construct. Central to this discussion was the distinction between variables and signals; you should know when you should SE each, and write PHD code

containing registers and signals correctly. We talked AIBO the “ wait” statement, and then ended the slide set with a discussion of level sensitive latches. Slide Set 6: In this slide set, we talked about tetchiness and non-synthesize PHD. We talked about several ways tetchiness could be used.

We showed that tetchiness can contain code to generate stimulus to a circuit (clocks, resets, general-purpose inputs). We also talked about how you can use a testament to monitor the behavior of your circuit and flag an assertion error when unexpected behavior is detected. It is important to remember that tetchiness can contain anesthetically PHD, since tetchiness are only used during simulation. Slide Set 7: In this slide set, we talked about various kinds to counters. There are lots of examples of synthesize VI-IDLE here, so it is good to review.

Be sure you know the various types of counters, and expect that you might be asked to design any of these counters, and in fact, design new types of counters that you might not have seen before (don’t freak out: if you understand these counters, you will be able to design anything new the exam [or your future boss] throws at you). Slide Set 8: In this slide set, we talked about four things. We first discussed “ types” in PHD. There are a number Of predefined types, and you can define your own types using records, arrays, enumerated types and/or subtypes. We then talked about “ for” loops.

As we discussed, most “ for” loops are not synthesize. The only way a “ for” loop can be synthesize is if the loop can be statically unrolled at run-time (so, the lower and upper bounds of the loop need to be known at compile time).

We then talked about “ generate” statements; these provide a short-cut for writing large structural designs. Finally, we talked about “ fighting” and showed how to design trip-state buffers, You should expect that you will have to design a circuit with a Tristan buffer in it. Slide Set 9: In this slide set, we talked about various implementation options, including Pass.

We discussed the difference between standard-cell design and full-custom design, and then described the differences (and advantages and disadvantages) between F-PAGAN and standard-cell design. We then looked inside an FAGAN to see where they get their flexibility, We examined how lookup-tables work and how they can e used to implement combinational logic. We also talked about the flexible routing structure that allows pins of logic blocks to be connected to each other, We briefly compared programming technologies and dynamic reconfiguration.

Slide Set 10: In this slide set, we looked at the internals off simulator. The key point was that your PHD is viewed as a collection of processes. The simulator “ runs” through your code by scheduling the execution through an event queue. This is reminiscent of how scheduling algorithms for parallel programming work (if you haven’t seen that before, you might next year). Slide Set I I: In this slide set, we talked about timing of synchronous digital circuits. From what you learned in this slide set, you can figure out the maximum clock speed Of any digital circuit.

We also talked about the set-up and hold-time flips-flops, as well as glitches. Finally, we talked about where immateriality comes from, and the implications of immateriality on design. Slide Set 12: Arithmetic Circuits: In

this short slide set, we talked about adders, subtract, and multipliers. We only talked about ripple carry adders this year. You should be able to describe how en is constructed and how it works, and estimate the speed or other resource requirements of a ripple carry adder. You should understand how an adder can be used to perform subtraction.

You should be able to talk about multipliers and understand how they work. Slide Set 13: Towpath Circuits: In this slide set, we talked about how real systems are usually divided into a towpath and control component. We looked a lot of examples that show how this is done. I won’t be expecting you to repeat the details of these examples on the exam, but you should be able to analyze or design simple systems consisting of both a towpath ND controller. Slide Set 14: Asynchronous Circuits: In this slide set, we first talked about Asynchronous State Machines. Loud expect that you can design simple asynchronous state machines, similar to the three examples we did in class. You need to remember to watch out for hazards, and do a state assignment intelligently. Besides that, is much the same as designing synchronous state machines, as you did in 2nd year. Slide Set IS is about asynchronous databases, and while the material is certainly fascinating, you wont find such questions on the final exam. This isn’t a complete list. But it Will give you a place to Start. You may be asked to write synthesize PHD.