Bistable flip-flop experiment

Objectives:

- To study the properties and performance of cross-coupled inverting logic gates.
- To set up the gates in order to obtain an experience, in the same time able to understand the Bistable Flip-Flop.

These circuits have been mostly replaced become a straightforward and effective design. These designs for applications including large dimension digital circuits. Although these circuits have been changed, they still have important use range, and it is necessary to understand their characteristics. This experiment state clearly that digital circuits are still be made from analogue parts. It has analogue functions correlative to current, voltages and time-varying diversification.

Materials and Equipment:

- Built-in socket connector bread board
- A selection of IC devices
- Jumper wires and connector leads
- Digital multimeter with test probes

Theory:

Flip-Flop

A standard Bistable circuit is made by simple combination of NAND gates or NOR gates. Hence, produce the required sequential circuit.

Common Sequential Logic circuits:

1. Clock Driven- Synchronized to a clock signal.

2. Event Driven- Asynchronous. Changing state when an external event happens.

3. Pulse Driven- Combination of Synchronous and Asynchronous.

SR NAND Flip-Flop

This system assembled of two inputs and two outputs. R and S inputs are representing Reset and Set. Q and are represent as outputs of the circuit. Firstly, user need to construct the inputs Set and Reset to a pair of cross coupled 2-input 7400 NAND gates in order to shape into a SR Bistable. Thus, the action of feedback may occur from each output to one of the other inputs.

RST Flip-Flop

The device connected and synchronized to a clock signal. The outputs are only trigger when Set (S), Reset (R), and Trigger (T) inputs are in logic 1 level. There will we un-trigger when the inputs are in logic 0 level.

NAND gate

- M74HC00 is a high rate CMOS QUAD 2-input NAND gate. Silicon gate C2 MOS technology is applied.

- The internal circuit is build up by 3 stages including buffer output, which can prevent high noise and produce stable output.

Task Discussion:

Investigation of a Bistable Flip-Flop

Theoretical Details:

The consequential circuit has two stable situations, when the direct feedback cross-coupling is implemented among inverting NAND logic gates. Bistable is either of which can be choose by submission of the correct input situation.

R and S inputs are representing Reset and Set. Q and are represent as outputs of the circuit. At standard running, both NAND inputs must normally be logic 1 level. The logic level of the Q and outputs will become relative.

To stabilizing the two possible states, changing the R input temporarily to logic 0 level, that will create a output with logic 1 level. In the same time, the output output with logic 1 level will be applied to the S input (2nd input), which is logic 1 level. Thus, the Q output will temporarily become a logic 0 level.

While both R and S inputs become logic 0 level at the same period, it is forbidden. In this state, both Q and outputs will become logic 1 level. Hence, that will override the load-back motion. The final state of the latch will not be resolved in front of time.

One practical unfavorable of the RS Flip-Flop effects from the data that the outputs can change state when either or both of the logic level of inputs is change. Operation is non-simultaneous.

Modifying the Bistable Flip-Flop: Creating an RST Flip-Flop

Theoretical Details:

It is similar in the RS NAND Flip-Flop operation. The R and S inputs are at logic 1 level. The third input (Trigger) has been added. The Q and outputs can only change states while the Trigger input is at logic 1 level. If logic level of Trigger input is 0, the R and S inputs are no effect for the outputs.

In a valid operation, the R or S inputs must be logic 1 level, and the Trigger input must be logic 1 level and then logic 0 level. In the end, the selected input must be returned to logic 0 level.

Investigation of a NAND gate

Theoretical Details:

The NAND gate is a digital gate, obtains voltages and currents at its inputs. While connect to the variable voltage supply, these may involve any value in a real circuit. For instance, since during an input changes, the output voltages may takes a non-zero time for the change to occur, so the voltages will not be accurately come up to 5V or 0V all the time.

Objective:

To concern the transforms and voltage levels of the output of the NAND gate to the states of the inputs.

Procedure:

1. Circuit shown in Figure 2. 7 is constructed and an external variable voltage from a power supply is used. Any value from 1k? to 10k? can be taken by R1.

2. A fixed digital voltage (0 or 5 volts) is applied to one terminal of a NAND gate. A variable voltage is applied to another terminal.

3. Firstly, the input voltage Vin is varied up to a maximum of +5V and Vin against Vout is plotted. Thus, the logic 1 output voltage (V1) and the logic 0 input voltage (Vgo) are determined.

4. The output unchanging for wide ranges of input voltage is noted.

5. To found the overall behavior, the rough initial experiment is did.

6. More reading is taken.

Conclusion:

All of the objectives are achieved. In this experiment we understand the theory of Bistable Flip-Flop, Standard SR NAND Flip-Flop and RST Flip-Flop. All of the properties and performance of cross-coupled inverting logic gates have been studied. Experience is obtained during the construction of the gates.

In conclusion, at standard running of SR NAND Flip-Flop, both NAND inputs must normally be logic 1 level. Thus, the logic level of the Q and outputs will become relative.

While both R and S inputs become logic 0 level at the same period, it is forbidden. In this state, both Q and outputs will become logic 1 level. Hence,

that will override the load-back motion. The final state of the latch will not be resolved in front of time.

For the operation of RST Flip-Flop, the Q and outputs can only change states while the Trigger input is at logic 1 level. If logic level of Trigger input is 0, the R and S inputs are no effect for the outputs. Hence, to obtain a valid operation the R or S inputs must be logic 1 level, and the Trigger input must be logic 1 level and then logic 0 level. In the end, the selected input must be returned to logic 0 level.

References:

- http://www. play-hookey. com/digital/rs_nand_latch. html
- http://www. play-hookey. com/digital/clocked_rs_latch. html
- http://us. st. com/stonline/books/pdf/docs/1879. pdf
- http://www. electronics-tutorials. ws/sequential/seq_1. html