

Silicon wafer

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The next step in the fabrication process is to create the buried channels by implanting phosphorous ions in areas that will eventually be covered by polysilicon gate electrodes. The n-type semiconductor formed by phosphorus contains negatively charged electrons as the primary charge carriers and forms a type diode structure, which serves to localize potential wells deep beneath the silicon/silicon dioxide interface. The potential well illustrated in the central portion of Figure 1 is a schematic drawing of the diode structure. The primary function of the buried channel is to localize integrated electrons away from the silicon/silicon dioxide interface, where they can become trapped during charge transfer. By localizing charge deep within the p-type silicon substrate, transfer of charge occurs more efficiently with a minimum of residual charge remaining in the gate.

After the buried channels are formed within the silicon substrate, a layer of silicon dioxide is thermally grown on the silicon wafer surface to provide an insulating base for the gate electrodes. Next, a phosphorus-doped layer of polycrystalline silicon (polysilicon) about 5, 000 angstroms thick is grown on top of the oxide layer. This layer of polysilicon comprises the gate electrodes (see Figure 1) and is transparent to visible light, making it an ideal substance for use in CCDs. Although the fabrication of a complete CCD takes additional steps, the basics of the MOS capacitor assembly have been completed at this point."

I Vs V Characteristics

(According to M. Aceves, O. Malik, V. Grimalsky V. 5 No. 2 (2004) P. 236-237), National Institute for Astrophysics, Optics, and Electronics (INAOE), Electronics Department.)

The dynamic I-V characteristics of these MOS structures when linear voltage
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sweep (60 v/ sec) was applied to the metallic semitransparent gate is shown in the diagrams below.

Dynamic I-V Characteristics of fabricated MOS capacitor with silicon dioxide as insulator with positive (above) and negative (below) charge recorded when a triangular sweep voltage (60 v/s) was applied to the gate.