Abstract:- johnson counter is also known as switched

Abstract:- Inthe latest designs of VLSI, power dissipation is a main advantage to reduce it. As technology is growing day by day our chip size is to be reduce, less timedelay and less power consumption of any system has become priority. In VLSI, sequentialCircuit takes a major part to optimizethe power and to reduce the chip size.

A counter is a sequential circuit havingmajor applications in microcontroller such that digital to analog converterssignal generators, digital alarm clock to computer memory pointers. In this paper low power, 4-bit Johnson Counter is to bedesigned by using clock gating Techniques. In this paper, we analyzed that theperformance of proposed Johnson counter is better than that of conventionalJohnson counter. Keyword–Johnsoncounter, clock gating, power dissipation, sequentialcircuit.

1. INTRODUCTIONCountersare very important part of digital system. It is widely used component indigital system. Counters are used to count the number of clock pulsessynchronously. Counter is a set of flip-flops that change their states in aspecific manner to generate a particular sequences. These sequences could beassociated with the number of times events can occurs.

Counters are based ontime that have constant and fast nature are required in designs of VLSI withhigh speed and to optimize the power. Counters are of synchronous type andAsynchronous type. Synchronoustypes of counter are important for providing different data series in asynchronous manner to a system. Johnson Counter is an importantpart in Digital to Analog converter, Johnson counter is one such counter systemwhich provides data

sequenceinitsdistinctmanner. In thispaper, we design a low power dissipation of Johnson counter using a clockgating Technique is described here.

As we know that continuous switching ofclock is the major supplier of power dissipation. Johnson counter is basicallya Ring counter with complement output of last shift register is feedback toinput of first shift register. Johnson counter is also known as switched tailring counter, twisted ring counter, walking ring counter. The basic differencebetween ring counter and Johnson counteris that Johnson counter is self started counter with initial value contained’0000′. 2. CLOCK GATINGClockgating is used to reduce dynamic power dissipation. It is used to block theunwanted clock pulse transitions where the output bit remains constant i. eoutput bits are not toggling the clock It Works by taking the enable conditionsattached to registers, and uses them togate the clocks.

There are two typesof clock gating styles available. They are: 1)Latch-based clock gating 2)Latch-free clock gating. 1) Latch-basedclock gating Inlatch based clock gating, it Uses a simple AND or OR gate. Glitches areinevitable i.

e. Glitch is any unwanted clock pulse that may occur during thetriggering of clock pulse. Thefigure below shows a flip-flop receiving a enable signal and a clock signal; ifthere is some glitch (unwanted change of state) in clock, it will take it as areal clock edge and latch the data to its output. However, if the pulse is toosmall, the data may not propagate properly to output and the flop may go metstable. It is less used. Fig: 1 Latch basedclock gating2) Latch-free

clockgating. Itadds a level-sensitive latch. It holds the enable signal from the active edgeof the clock until the En D Q inactive edge of the clock D Q It produced lessglitch CK Gated CK clock.

It Easy adoption by EDA tools. Fig: 2 Latch freeclock gating. 3. CONVENTIONAL JOHNSONCOUNTERInthis section, the design and output of conventional Johnson counter isdescribed. Johnson counter is nothing but a ring counter with its last outputbeing inverted and fed to the input at first Flip-flop. D or J-K flip flop inmaster slave configuration are used in the Johnson counter to shift the datasynchronously as per the output sequence of the counter.

The output countingpattern of Johnson counter is shown in the table described below (Table. 1). Clock pulse Q3 Q2 Q1 Q0 1 0 0 0 0 2 0 0 0 1 3 0 0 1 1 4 0 1 1 1 5 1 1 1 1 6 1 1 1 1 7 1 1 0 0 8 1 0 0 0 Table: 1Output pattern of 4-bit Johnson counter. 4. POWER CLOCK GATED DESIGNInthis section, clock gated Johnson counter is explained which eliminated the numberof inputs. Hence, power is reduced. A clock gating logic comprises between logic gates.

5. SIMULATION RESULTTheClock Gated Johnson counter has been designed. The output waveform is shownbelow. The circuits are simulated using Xilinx 14. 1 simulation tool. Simulations are done on the time delay 0.

01ns. 6. CONCLUSION The proposed design shows reduction in thepower of the design which has clockgating logic in it. Due to the use of clock gating we have achieved a powerreduction. REFERENCES1SaniMd. Ismail, Mohd.

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