Anodic (dokmeci and kirkos 2001), capacitive micromachined

Anodic bonding is a technology ofhermetical bonding of glass and silicon wafers. It is widely used in sensingmicroelectronic devices. Silicon and glass wafers are bonded together underhigh temperature (usually in the range of 300 C to450 C) andsimultaneous voltage application (up to 1000 V DC). After coolingto room temperature, this silicon–glass stack has residual stresses due tothe thermal mismatch of glass and silicon. Such stress can be seen as aresult of bonded wafers bowing.

Decreasing the effects of thermal mismatchstress can improve the reliability of microelectronic devices produced usinganodic bonding technology. It is important for such devices as micromirrordevices (Dokmeci and Kirkos 2001), capacitive micromachined ultrasonictransducers (Xu, Yu, and Yu 2011; Walter, Bourbon, and Moal 2014), andmicromachined vibratory rate gyroscopes (Hou et al. 2011).

There is alsoa study (Harz and Engelke 1996) of decreasing such stress byadditional heat treatment causing structural relaxation of the glass. In this paper, we report the theoreticalstudy and estimations of thermal mismatch stress reduction by proper selectionof bonding temperature and glass thickness. This can be done only after priorthorough study of the temperature dependence of the linear thermal expansioncoefficient of used glass.

We show by analyzing such dependence of fourglass brands known to be bondable to silicon that the usual thoughtof decreasing the bonding process temperature as a solution to thermalmismatch stress can be a failure. Materials and methodsOur analysis is based on estimates ofresidual stress

by two mathematical models. We use the following assumptionsfor both models:• Glass and silicon layers areinitially (just after bonding at the bonding temperature)undeformed.• Both layers are homogeneous andperfectly elastic.• Temperature of both layers isthe same and is uniform. The first model we use is essentiallya model for thin-film stress, but unlike the equations shownin Refs.

and , it uses integration of the linear coefficient ofthermal expansion (CTE) difference between the bonding temperature and working temperature . We willfurther refer to this model as the simple modelwhere is the residual stress in silicon due tothermal mismatch (Pa); is the temperature of the anodic bonding process (K); is the working temperature (K); , are the Young’s moduli of silicon and glass, respectively (Pa); , are the thicknesses of silicon and glass, respectively (m); , are the linear thermal expansion coefficientsof glass and silicon, respectively (K). We usethis model with the following assumptions:• Plane sections remain plane.• Glass and silicon layers areinitially undeformed.

• Strains and stresses for eachlayer are assumed to be equal to those near the glass–silicon interface. The second model is based on thehypotheses of the classical lamination theory (CLT) of plates with applicationto hygrothermoelastic problems in composite laminates. It is thoroughlyformulated and discussed in Refs. and . We use integration of CTEacross the range between bonding and working temperatures in this model, too. Bonded silicon–glass plate is considered to be a laminated plate with twolayers (in this study): silicon and glass. Each layer has its own thickness andthermomechanical properties.

We will further refer to this modelas the advanced model. We use this model with the followingassumptions:• The plate thickness is verysmall compared to its length and width.• Stress state of the plate isassumed to be the plane stress.• Glass and silicon layers areperfectly bonded together.

• The normal to the middlesurface is assumed to remain straight and perpendicular to the middle surfaceof the plate.• Strain, perpendicular to themiddle surface, is ignored. For the purpose of this research, weuse polynomial approximations of measured CTE of glass brands known to bebondable to silicon. See Table tab: results_approx_ctefor the polynomial coefficients used. Two borosilicate glasses' brandsapproximations, Borofloat 33 and LK5, were published previously (Sinev andPetrov 2016). Two others, of borosilicate glass Corning 7740 andalumosilicate glass Hoya , were obtained by the same procedure. The temperaturerange was from 170 to 780 K (from 100 C to500 C). Foreach glass brand, there were three samples cut out from a single wafer.

Resultsof these samples were averaged. For each sample, there were 20 experimentalpoints measured. Force applied from the quartz probe to the sample placed inthe quartz column was 0. 2 N. Measurements were done while increasing thetemperature with a 10 K/min rate. All estimations to be discussed furtherwill be based on this data.

Mechanical properties of {100} orientedsilicon were taken from Ref. , p. 42. The linear thermalexpansion coefficient of silicon can be found in Ref. . It

isindependent of the crystallographic orientation as in a cubiccrystal (Slack and Bartram 1975). See Fig. fig: cte_graph_measured for a graphicalrepresentation of the temperature-dependent CTEs used in this paper.

tab: l Stable-format=-1. 3Stable-format= 1. 3 Stable-format=-1.

3 Stable-format= 1. 3 @ Glass brand & , 106 K1 & , 108 K2 & , 1011 K3& , 1014 K4Corning 7740 & 2. 893 & 0. 500 & -1. 231 & 0. 740Schott Borofloat 33 & 1. 628 & 1. 040 & -2.

198 & 1. 398LK5 & 1. 123 & 1. 607 & -3. 496 & 2. 435Hoya & -0. 193 & 1.

453 & -1. 847 & 0. 910fig: cte_graph_measuredCTEs of discussed anodic bonding materials. Unless otherwise noted, we use a siliconwafer of 460-m thicknessand a glass wafer of 600-m thicknessfor our estimations. Results and discussionAnalysis of models and modelingresults showed that thermal mismatch residual stresses in two-layeredstructures without cavities are proportional to the integral of the CTEdifference between the glass and silicon usedwhere is the residual stress in silicon due to thethermal mismatch (Pa); is the temperature of the anodic bondingprocess (K); is the working temperature (K); , are the linear thermal expansion coefficientsof glass and silicon, respectively (K). In the simple model, stress changes itssign (tensile or compressive) only with changing of a layer (silicon or glass)where stress is estimated. The value of stress will be determined by aproportional coefficient depending on the mechanical properties of silicon andparticular glasses and the proportion between wafer thicknesses.

fig: sigma_workt_4glasses_simpleResidualstresses in silicon bonded to different glasses estimated by a simplemodel. fig: nakop_deform_ofworking_graphRelativedeformation at wide range of working temperatures of silicon–glass bonds. fig: nakop_deform_ofbonded_graphRelativedeformation at 20 C ofsilicon–glass bonds made at different temperatures. See Fig. fig: sigma_workt_4glasses_simplefor an estimation of the residual stress at a wide variety of workingtemperatures in silicon bonded to different glasses at severaltemperatures. One can see that each glass has its own influence on the stressvalue in silicon with changes of the bonding temperature. An increaseof the bonding process temperature causes an increase of the tensilestresses in silicon (according to a simple model) for three of fourglasses estimated, the exception being Hoya . Due to differencesin CTEs (especially the temperature of intersection with the silicon CTE, see Fig.

fig: cte_graph_measured), stresses caused by LK5 are more compressive and, at the same time, are lessinfluenced by changes in the process temperature compared to those byBorofloat 33 and Corning 7740. Estimation for stress at 20 C insilicon bonded to Corning 7740 at 310 C in thiswork is in good agreement with warpage measurements of silicon to glass wafersbonded at similar temperatures measured in Ref. (0. 017 mm bowfor = 340 C and evenless with closer to 310 C). Variations of the bonding temperature for Hoya cause lesser changes in stressafter bonding as compared to changes in the stress of silicon bonded to borosilicateglasses. As can be seen in Fig.

fig: sigma_workt_4glasses_simple, the general thought that “ higher silicon–glass anodic bonding processtemperature causes higher residual stress” is applicable only to certainglass types or even batches of glasses as the thermal expansion coefficients ofglass may vary from batch to batch. One can also see that the statement” there is a temperature which provides a no-stress bond” (Cozma andPuers 1995) can be true only at selected working temperatures. As the devicesproduced are usually working in some temperature range, they will have varyingthermal mismatch stresses at variable ambient temperatures. fig: glass_stress_multilayerEstimation by advanced model of residual stresses in silicon–glassbond at 20 C that wasmade at 300 C comparedto FEM results. Stresses were estimated along (100) direction of silicon. axis with zero at silicon–glass interface, andperpendicular to it with positive direction towards unbonded glass surface. One can compare glasses by thedifferences in accumulated strains of silicon–glass bonded samples both in aworking temperature range and in a bonding temperature range. This can be doneafter measuring the temperature dependence of their CTEs in the range betweenthe lowest working temperature and the highest allowable temperature either forthe anodic bonding process or for the whole device fabrication process.

Asshown in Figs. fig: nakop_deform_ofworking_graph and fig: nakop_deform_ofbonded_graph, graphs are made by evaluation of the integral part of Eq. (eq: stress_prop_to_nakop_deform). Note that, according to our estimation, LK5 glass bonded to silicon at420 C causesalmost the same residual stresses as Corning 7740 bonded to silicon at310 C. fig: glass_stress_multilayer_ot_h_twEstimationby advanced model of residual

stresses at free side of silicon layer atseveral working temperatures. Bonding temperature for both glasses is 300 C. fig: glass_stress_multilayer_ot_h_tbEstimationby advanced model of residual stresses at free side of silicon layer at severalbonding temperatures. Working temperature for both glasses is 20 C.

In the advanced model, the sign of stressat a particular depth in silicon–glass laminate depends on the proportionbetween wafer thicknesses (see Fig. fig: glass_stress_multilayer). Stress in silicon varies in sign and value as glass layer thicknesseschange. As can be seen in Fig. fig: glass_stress_multilayer, simply interchanging one glass brand to another without changing the bondingtemperature can produce inverted results in residual stresses cases. These results are in good agreement withfinite-element modeling (FEM) simulated by Coventorware (modeling softwarebased on ABAQUS).

The models used consist of two merged and meshed layers: silicon and glass. Each layer is a circle plate in the -plane withthe -axisperpendicular to its diameter. Both layers have the same diameter of100 mm.

The silicon layer has a 0. 46-mm thickness and the glass layer hasa thickness of either 0. 6 or 2.

5 mm. The mesh type was set to be “ extrudedbricks” (hex-dominant algorithm with linear element order) with an elementsize of 3. 5 mm, minimum element size of 0. 35 mm, and element size inthe extrude direction of 1/10 of each layer thickness. Each material was set toa zero stress temperature of 300 C and theCTE for material was recalculated according to the software instruction manual.

Then the temperature of modeling was set to be 20 C (as avolume boundary condition). A thermomechanical nonlinear solver was used with” fixZ” surface boundary condition applied to the edge formed by theintersection of free glass surface and the diameter of the glass layer. Datafor FEM stress shown in Fig. fig: glass_stress_multilayerwere averaged from points inside a cylinder with a radius of 3. 5 mm in acentral zone of 100 mm bonded wafers.

The advanced model shows that for eachsilicon wafer thickness there is a particular glass wafer thickness , whichprovides a no-stress state at the free side of the silicon layer independent ofthe bonding or working temperature. The estimated proportion together with the glasses’stiffness is shown in Table tab_h0_stekla. Figures fig: glass_stress_multilayer_ot_h_tw and fig: glass_stress_multilayer_ot_h_tbshow that for Schott Borofloat 33 and LK5 glasses bonded to solid siliconproportion of thicknesses / that minimizes residual stress at unbondedside of silicon wafer is close to 3. The lower the glass stiffness, the higherthis number.

Considering this, we suppose that by varying the thickness of theglass wafer to be bonded to a silicon wafer, one can achieve the desirableresidual stress value and sign at the silicon surface where sensing elements ofmicrosystems are usually situated. tab_h0_steklaEstimated proportion of glass waferthickness to silicon (both wafers without cavities), which provides a no-stressstate at free side of silicon. Glass brand , GPa Corning 7740 62. 75 0.

200 3. 12 Schott Borofloat 33 64. 00 0.

200 3. 09 LK5 68. 45 0. 184 3. 05 Hoya SD-2 86. 89 0.

244 2. 54 ConclusionTheoretical estimation of residualstresses due to thermal mismatch between anodically bonded silicon and severalbrands of glass has been conducted. Two models were used: thin film stress, anda model based on the CLT of plates. Integration of temperature-dependent linearthermal expansion coefficients of glass and silicon across the range betweenbonding and working temperatures was used in both models. Study showed that residual stresses dueto thermal mismatch between anodically bonded silicon and glass can be reducedby justifiable selection of the bonding process temperature and glassthickness.

Structures produced by silicon–glass anodic bonding will havevarying thermal mismatch residual stress at variable ambient temperatures. Byvarying the thickness of the glass wafer to be bonded to the siliconwafer, one can achieve the desirable residual stress value and sign at thesilicon surface where sensing elements of microsystems are usually situated. For studied borosilicate glasses, the desirable glass to silicon thicknessproportion is approximately of value 3.

Obtained results are in goodagreement with FEM done by us and experiments conducted by other researchers inthe past. Though this study can be of greatimportance to microsystem developers, further research of thermal mismatchstress estimation of highly structured silicon wafers bonded to glassis a demanding task.