

The effect of the esd information technology essay

Technology, Information Technology



ABSTRACT

Electrostatic discharge (ESD) costs the electronics industry millions each year in damaged components, non-functional or malfunctioning circuit boards and scrambled or missing information. ESD can occur during manufacturing, shipping, receiving and field handling of integrated circuits or printed circuit boards with no visible signs of damage. ESD is a transient discharge of static charge accumulated on a human body, a test device, or a chip through a low-impedance path due to either human handling or a machine contact. Currents during the ESD events become quite high, but are in nanoseconds time frame. Part of the component is left permanently damaged by this, which can cause two types of failure modes: catastrophic damage or latent failure. Catastrophic leaves the part completely nonfunctional. Latent failure can be much more serious, allow the problem component to work for hours, days or even months before resulting in catastrophic failure. If such components end up in critical applications, such as medical, military, space then the consequences can be grim. A significant ESD event will generate electromagnetic interference (EMI) that can be destructive to neighboring electronic systems. A high energy ESD can drive substantial EMI energy to couple and charge passive circuits or energize active circuits resulting in significant system problems. This can manifest itself in the form of logic error conditions including data errors, systems lock-ups, malfunctions and software errors. A device, circuit or a system that is susceptible to ESD will respond to the discharge in different ways depending on a number of factors, which include the location of discharge, voltage level of discharge and environment in which an ESD event occurs. It has now become increasingly

more important for all manufacturers plus the users of integrated circuits and other electronic components to fully understand the nature of ESD, sources of ESD, protection against ESD and impact on quality and reliability. There is a trend toward greater ESD susceptibility as integrated circuit (IC) technologies achieve higher speed, smaller geometries, lower power and lower voltage. When these ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Thinner gate oxides, complex chips with multiple power supplies, mixed signal blocks and faster circuit operation all contribute to increased ESD sensitivity of advanced semiconductor products. The amount of energy needed to damage metal oxide semiconductor (MOS) devices is scaled down with technology; however the level of ESD stress generated due to either human handling or device contacting remains unchanged. So the modern complementary MOS circuits are much more vulnerable to ESD stress. Since people are considered to be a prime source of ESD, ESD test circuit is based on a human body model (HBM). An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical specifications. Common ESD failures are caused by either thermal breakdown in silicon and/or metal interconnects due to high current or dielectric breakdown in gate oxide due to high voltage overstress. To protect circuits from ESD induced damage, ESD protection devices must provide a low impedance path that bypasses the circuits under protection during an ESD event and discharges the static charge to the ground before it damages the protected circuits. It is important that ESD robustness be given the same level of priority as the circuit performance.

Research Objective

This research work concentrates on the direct and indirect discharge effects of ESD on the working of the devices, circuits and systems. The implemented work comprises of experimental verification of failure and malfunctioning of integrated circuits and electronic components to low rise time ESD transient pulse. Results regarding soft or hard failure and malfunction have been reported for various ICs, circuits and systems. Learning from the failure aspects of the devices, circuits and systems tested for ESD, a clear idea is obtained on how to design a system which can withstand ESD stress test to a tolerable standard level. A system has been designed with standard board design rules implemented and ESD protection devices incorporated which has been tested as per IEC 61000-4-2 ESD system level standard. The objectives of the proposed Research include the following: Mathematical analysis and simulation to calculate the induced voltage in cables due to ESD radiated fields. To model the radiated susceptibility of electronic subsystem to ESD. To analyze the effects of ESD and find mechanisms to reduce ESD susceptibility of devices, circuits, systems and complex electronics. To evaluate the effect of ESD on custom designed microcontroller systems implemented using standard board design rules and protection devices. A coupling model has been developed to estimate the induced voltages at terminations in unshielded cables for radiated fields generated due to ESD. In case of unshielded cables, RC shunt terminations are preferred over resistive and CMOS device terminations as the induced voltage is in the mV range. A Generic program in Visual C++ to compute the induced voltages for varying parameters of the current waveform, length, height of the cable and

angle of incidence has been implemented. This can also be used to calculate induced voltages for different cable configurations. Using MATLAB, the data imported from Visual C++ is used to calculate induced voltages. It has been observed by simulation that in shielded cables, the voltages induced due to radiated ESD is negligible thereby reinforcing the theory that shielded cables can protect equipment from high frequency radiated fields due to ESD. The induced voltage and current in the center conductor due to ESD generated fields is larger for a braided cable when compared to a non-braided cable. This analysis will estimate the transient voltages appearing at the input of the system connected to the coaxial cable. This estimate can be used to develop appropriate mitigation techniques to protect the sensitive system that is connected to the shielded cable. Radiated susceptibility analysis is carried out for an electronic subsystem. MATLAB is used to model the response of very high frequency (VHF) amplifier to ESD generated radiated electromagnetic (EM) fields. It is observed that a greater part of the energy due to ESD simulation currents has frequency components extending to the VHF and UHF bands. So the VHF amplifier is susceptible to ESD events in this frequency range. If the distance between the ESD generator and the pickup antenna is decreased, the peak magnitude of the voltage coupled to the amplifier input terminals increases. The amplitude of the fields at antenna terminals, open circuit voltage at antenna input terminals, voltage at the input and output of the amplifier decreases sharply with increase in distance from ESD source. It has been observed from simulation that the induced voltages at the amplifier input terminals can be as high as 7.446 V with a rise time of approximately 1 ns for a distance of 0.5 m between the ESD

generator and the pickup antenna. This can cause malfunction of the electronic circuitry inside the amplifier. The spice circuit modeling with transient analysis concurs with the experimental results for air discharge on analog circuits. The zero crossing detector is more susceptible to ESD when compared to the RC phase shift oscillator. The oscillator circuit using discrete components takes some time to come back to its initial working condition after the ESD discharge, but the detector circuit using opamp got damaged by 15kV of air discharge voltage. Higher discharge voltage and shorter distances produce larger transients and distortions in analog circuits. The digital switching circuit without decoupling capacitors at Vcc malfunctioned when an ESD event occurred at a distance of 35 cm from the circuit. Post discharge analysis revealed that Binary counter IC SN74LS393N had failed functionally. The importance of adding decoupling capacitors to the supply point of each of the ICs is verified. The response of the data to ESD in a digital switching circuit with decoupling capacitors at Vcc depends on the position of trigger or instance of occurrence of the discharge. The distance at which the pulse is discharged plays an important role on the amplitude of the transient. The discharge on Vertical coupling plane (VCP) affects the digital data more than the discharge on Horizontal coupling plane (HCP). Smaller the value of decoupling capacitor, the more susceptible the digital circuit becomes to ESD. The logic gates like NAND, AND, OR, XOR and Inverter belonging to both the transistor-transistor logic (TTL) and CMOS logic family are subjected to pin to pin ESD stress. Experimental investigations of the TTL and CMOS logic gates reveal that CMOS devices are more susceptible to ESD than TTL devices due to the presence of a dielectric

media in the case of CMOS devices which can easily breakdown for high voltages. The effect of ESD on grounding in a mixed mode circuit is studied since the analog signals are more sensitive to noise from the digital circuits. It is observed that the analog output is affected less by transients when the analog and digital grounds of the mixed mode circuit are separate. The effect of the ESD on the MC9S08QE128 8-bit microcontroller circuit is analyzed. The hardware circuitry has been configured to act like a diagnostic tool, indicating an error if the hardware fails. The 8-bit microcontroller has only in-built, on-chip ESD protection. Direct air discharge at 12kV twice on the connector GPIO pins resulted in the shorting of power rails VDD and VSS of the microcontroller which in turn ended in the thermal shutdown of the microcontroller and the failure of the designed tests. System level test has been conducted on the 16 bit microcontroller MSP-EXP430G2 Launch Pad Development Board where all IEC specified system-level failure criteria classifications are observed. The launch Pad soft or hard resets in majority of the ESD stress it is subjected to, owing to its careful design and ESD considerations. A contact discharge of 8kV to the Rx-Tx pins of the jumper array damaged MSP 430G2231 IC. The microcontroller MSP 430G2231 is found to be not communicating with the software and the program is not executable. Custom designed four layer boards with 32 bit microcontroller interfaced with various components like the UART, audio interface, USB and the LCD display and key matrix are developed. All the standard design rules for PCB are followed in the case of the microcontroller test boards: one populated with devices having in-built, on-chip protection and the other board with extra off-chip, on-board protection devices. The board with devices

having on-chip protection is affected by ESD with problems like malfunction, reset and damaged interface module. The board with on-board protection devices like ferrite bead, capacitors and TVS diode is hardly affected by ESD and the interface modules are also functioning normally in this board. ESD susceptibility tests on complex electronics devices such as Field Programmable Gate Arrays (FPGA) and Complex Programmable Logic Device (CPLD) are conducted. Direct air discharge tests are performed on the insulators in the FPGA/CPLD kit like the seven segment display; liquid crystal display (LCD) and flat ribbon cable (FRC). Direct contact discharge tests are performed on the metal points like the switches, I/O pins and the mounting screws of the FPGA/CPLD trainer kit. ESD tests and failure analysis reveals that FPGA and CPLD are very sensitive to ESD and there is damage to FPGA3s50 IC and CPLD 9572 IC. Exhaustive mathematical modeling for cables and simulation of radiated susceptibility of electronic subsystem is carried out. Characterization of conducted susceptibility due to ESD on integrated circuits and electronic components in various designed analog, digital and mixed mode circuits; systems such as 8-bit, 16-bit and 32-bit microcontroller units interfaced with various devices and complex electronics such as FPGA/CPLD devices is carried out. The methods presented are useful in estimating the transient voltage levels that may be appearing at the terminals of electronic equipment and at the board levels a priori. This can be used to devise protection circuits and schemes to protect the systems according to international standards.