The effective use of miller's indices of importance in technology

Media, Social Media

Give two examples

Answer 1: According to the class lecture and YouTube video by Patrick Shamberger (Indexing Crystal Planes using Miller Indices {Texas A&M: Intro to Materials (MSEN 201)}) supplied in this homework question, Miller indices can describe the position of an atom by coordinates in a crystal, and describe how atoms are repeating in the crystal structure. This form of crystallographic notation in three dimensions h, k, l is of interest to analyze and describe atomic orientation since different chemicals can remove different atoms via etching. Miller indices can be used to designate planes and directions in a crystalline lattice which repeats and gives vector representation for the atomic plane orientation in the lattice, and can be defined as reciprocals of the fractional intercepts the plane makes with the crystallographic axes. Thus, Miller Indices are important in their usage to index crystallographic planes, helping to describe a plane for its boundaries, surfaces, etc. in crystal structures. For example, we can use Miller indices to describe planes in silicon.

The (100) plane and (111) plane produce an angle of 54. 74 degrees. Silicon can be cut at this 54. 74 degrees via chemical etching to produce very flat plane used for MEMs. Properties of silicon also vary for each miller orientation index: For example, 100 plane is the weakest plane as it has least number of atoms. 110 plane has cleanest surface in micro fabrication, and 111 plane has shortest bonds between atoms so it is the strongest plane to work with. Another example, as discussed in the video, Miller indices can be used in regards to describe Marten sites in martensitic structure, as twinning can be observed along specific crystallographic planes, or, one can be interested in locating/describing grain boundary interface separating neighboring but uniquely oriented crystals. In terms of practical examples, in a general triclinic axis, as a special case, intersection can be at infinity if the plane is parallel to the axis of interest. So, when taking the inverse of that, the miller notation would be 0 for that particular axis.

Czochralski method: Why do we want to make big wafers? Can the Czochralski method use compound semiconductors? GaAs? InSb?

Answer 2: A larger diameter silicon wafer can hold more microchips and allow for more volume of production and semiconductor devices from 1 wafer for electronics for more market value. As for compound semiconductors, the standard Czochralski method is most suitable for one element systems for single crystals of semiconductors, metals, etc. , such as high purity silicon. Compound semiconductor Gallium arsenide (GaAs) has two components, however, according to J. Friedrich, a single crystal bond of Gallium arsenide (GaAs) can be grown with Liquid Encapsulated Czochralski method (LEC) where elemental Ga and As are put in a crucible with boric oxide/boron trioxide which acts to prevent the evaporation of volatile component like arsenic.

There are conditions of the pressure of the inertial gas in the growth chamber exceeding partial pressures of volatile components (J. Friedrich 2016), although the Bridgman method is optimal for GaAs since a two part furnace is used, one to prevent arsenic loss and the other to keep polycrystalline GaAs above melting point—both methods are however still limited by crucible contamination(Like Boron) and melting defects (Barron 2013). Indium antimonide (InSb)can be used as a compound semiconductor material with Czochralski method; J. A. Godines et al. were able to use the Czochralski method to produce InSb single crystals with an etch pit density of 3. 8 × 102 cm−2 (Godines et al. 1997). Method wise, according to Galaxy Compound Semiconductors, Czochralski can be used for single crystal InSb boule up to 150 mm diameter, where first high purity In and Sb are placed in a growth crucible with an inert atmosphere and a steady addition of Sb to the melt during pulling, Te for doping, and then seed crystal of InSb is rotated and slowly withdrawn from the melt and crystal necking applied (Galaxy Compound Semiconductors Inc. 2018).

Si on SiO2 A technology of importance. Find what is it? What can you use it for – 2 examples

Answer 3: According to class lecture, Si/SiO2 wafers can be microfabricated from the formation of a layer of SiO2 on the surface of silicon via thermal oxidation at 900-1200 C with oxidant source, using either a dry(oxygen-nitrogen) method or wet(water vapor) diffusion method. When SiO2 is deposited onto the bare silicon by the oxide diffusing in, one portion of silicon is converted in volume to SiO2, in which volume of SiO2= 2. 17*(volume of Si consumed), and the oxide thickness can be measured with ellipsometry. According to Nanografi, in most silicon- based devices, the SiO2 layer + Si can have usage as a doping barrier or usage as a dielectric layer to act as an insulator(Nanografi). Also, according to SVMI, two important usages of Si/SiO2 include use as dielectric material as well as in MEMS-related devices – for example, they state that wet thermal SiO2 + thick film Si can be used as part of a technique for chemical mechanical planarization for polishing tools (SVMI). SVMI states this concept is of a 3 layer stack SILICON ON SIO2 INSULATOR WAFER design, made up of Si on SiO2 which is also on a third layer defined as silicon wafer. This design can be fabricated by wafer bonding or SIMOX oxygen ion beam implantation and is stated to be applicable for MEMs and CMOS integrated circuit fabrication, used to reduce power and heat, and also used to enhance device speed performance (SVMI). This technology designis better known as Silicon on Insulator (SOI), where silicon wafer is above a silicon dioxide electrical insulator; this technique allows for usage in the computer industry such as for AMD 8 core microprocessors or processors in video game consoles (Chip Architect 2000). Alternatively, to produce affordable biosensors, Kai Sun et al. demonstrated that a thermal SiO2 layer could be grown on silicon wafer that was then anisotropically dry etched and subjected to silicon layer deposited on top of SiO2 and patterned via photolithography to form amorphous Si nanowires(Sun et al. 2011).