

Motivation and objective of the thesis engineering essay

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1. INTRODUCTION

As advances in lithography and fabrication of N-type Metal Oxide Semiconductor (NMOS) technology became possible in the 1970s, the bipolar digital logic, transistor-transistor logic (TTL) are obsolete in digital design world for exactly the same reasons that caused older technologies, such as the vacuum tube technology are lost. The performance of Integrated Chip (IC) doubles in every eighteen months whereas, interconnects performance doubles in next decade. This mismatch of development is due to capacitive and inductive effects poses in the design of VLSI systems. The power dissipation, delay and crosstalk problems are the major issues to be handled and are very much dependent on frequency of signal used, length of interconnects, transitions and present as well as previous pattern of data in line etc. The most obvious way to connect functional blocks in SOCs is to have a dedicated link between every component. A wide variety of networks exist between fully connected network and a shared path bus. The more complex interconnection architectures are sometimes needed in system design. These include hierarchical buses and also interconnections not based on a shared path such as crossbars. Examples of relatively complex interconnections used in SOCs include circuit switched networks, packet switched networks, and combinations of these two. Due to dominating nature of interconnect area, a shared path interconnect, i. e., a bus is a good choice for on-chip interconnection. The shared interconnect path minimizes silicon area requirement. This is mainly due to three factors: bus-based systems have a long history in computer system design, different parts of the system can be designed in isolation from each other, and bus protocols

are usually quite simple. Bus-based interconnects typically have signal lines for address, data, control, interrupt, and error signaling. In addition, they usually have a common handshaking scheme and means for arbitration to resolve bus ownership. In today's UDSM designs, the interconnect wires play a major role in the timing behavior of logic gates and in the power consumption of large Systems-on-Chip (SoC). The main reasons are the relative scaling of cell capacitances and, the thinner and more aggressive metal pitch of modern technologies causing the increase of inter-wire, or coupling capacitances. The latter effect, in particular, is increasingly important in technologies below 90nm, in which coupling capacitances between adjacent wires become significantly larger than the capacitance between a wire and the substrate, known as the self capacitance. The coupling capacitances are very important mostly because they affect wire delays, transitions to opposite values on adjacent wires will exhibit longer delays than for other types of transitions, in addition, the delayed transitions are often preceded by spurious spikes. These effects are commonly grouped under the term crosstalk. Increased coupling capacitances, however, are also critical for power consumption, because for some types of transitions will cause these large coupling capacitances to switch, and the spurious transitions will also dissipate unnecessary power. Coupling effects are particularly critical in long, cross-chip buses, because of the large capacitances due to their length, and also because conventional routing algorithms tend to keep bus wires close together, thus increasing the number of adjacent wires categorizes the worst-case crosstalk patterns that may occur among three adjacent wires and cause the increase of the

propagation delay. In the best case, when the three wires are switching in the same direction, the delay on the victim wire is the delay without crosstalk. However, the bus clock cycle must be adapted exclusively regarding the worst case delay to ensure the integrity of the transmitted data. The power consumption is roughly proportional to the percentage of appearance of the worst-case transition patterns. The performance of a high-speed chip is highly dependent on interconnects, which connect different macro cells within a VLSI/ULSI chip. With the continuous trend of Very Large Scale Integration (VLSI) technology scaling and frequency increasing, interconnect delay, crosstalk and power consumption become a significant criterion for evaluating performance of system. It is a result of increased resistance, capacitance and inductance of interconnect in the nanometer technology. From International Technology Roadmap for Semiconductors (ITRS) projection, interconnect delay and power can contribute to more than 50% of the delay and power when feature size is beyond 180 nm. The power and delay is an important factors to be considered while developing the algorithm/technique for better transmission.

1. 2 INTERCONNECT PARAMETERS

An IC's would be non-functional without wires connecting all devices on the die. When we connect two circuit nodes in a circuit schematic, we assume that it as an ideal wire without any delay or attenuation. But, real interconnects have a resistance, capacitance, and inductance per unit length making the wire an unintended parasitic circuit element. Early IC implementations were running at low frequency and the impact of parasitic capacitances associated with transistors dominated over the ones referred to

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interconnect. These early processes typically had two metal layers and one poly-silicon layer available for interconnect routing. Increased integration and chip complexity lay the foundation for more interconnect layers. Future state-of-the-art processes are expected to have over ten metal layers where low, thin, tight layers are used for local routing and high, thick, sparse layers are utilized for global interconnect and power. Wire lengths tend to increase in today's multi-GHz ICs. Signals are transmitted with fast rise times across global low resistive copper interconnects with large cross sectional area, surrounded by insulators with low dielectric constant. The interconnect has become a dominant issue in high performance ICs, the focus of the circuit design process has shifted from logic optimization to interconnect optimization. Multiple criteria should be considered during the interconnect design process, such as delay, power dissipation, noise, bandwidth, and physical area. Extraction and understanding of the parameters of interconnect is important for estimation of interconnect behaviors. The basic parameters are same as the parameters of the transmission line as resistance, capacitance and inductions. The other behavior parameters also arises due to the interconnect resistance, capacitance and inductance. The parameters that affects the interconnect behaviors describe in later subsections.

1. 2. 1 Interconnect Capacitance

Interconnects are a form of strip of metal over a return ground plane, as shown in Figure 2. 6. w , h , and d is the wire width, height, and length, while t_{ox} is the distance to the underlying ground plane. An electric and magnetic field is created around interconnect if a driving circuit injects a voltage and

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current signal, respectively in interconnects as shown in Figure 1. 2. When two conducting objects are charged to different electric potentials, an electric field is created between them and a capacitance, C , arises. It always takes some non-zero time to build up a voltage between two objects. The capacitance can be seen as the reluctance of voltage to instantaneously increase or decrease in response to an input signal. The capacitance for the single isolated interconnect wire in Figure 1. 1 can be approximated by Eqn. (1. 1)....(1. 1)Where, C_{pp} is the " parallel-plate" (bottom area-to-substrate) capacitance, C_{fringe} is the fringing (side-wall-to-substrate) capacitance, and ϵ_{ox} is the insulator dielectric constant. Figure 1. 1: Single Micro-strip Wire Figure 1. 2: Fringing Capacitance A wire is surrounded by a large number of other wires on the same layer and adjacent layers of the multilevel interconnect hierarchies. Each wire is coupled not only to the grounded substrate, but also to neighboring wires, as shown in Figure 1. 2. Eq. 1. 4 is not a good model for the capacitances of a wire in such a complicated three-dimensional interconnect structure. In fact, as technology is scaled, the denser inter- layer and intra-layer routing in modern processes makes inter-wire capacitances equally or more important than parallel plate capacitances. This effect is more notable in higher metal layers since interconnect is routed farther away from the substrate. The nearest neighbors are considered for analysis of behavior due to the short-range nature of electrostatic interaction. Interconnect capacitance is composed of two components, the capacitance between the interconnect and adjacent metal layers or substrate C_g , and the coupling capacitance between neighboring interconnects in the same layer C_c . C_c is expected to dominate

C_g in the DSM regime due to the increasing aspect ratio and decreasing wire spacing. Using the basic geometry, parallel plate capacitance, C can be calculated. When a wire thickness is comparable in magnitude to ground-plane distance (t_{ox}), fringing electric fields significantly increase the total parasitic capacitance is given by Eqn. (1. 2) and Eqn. (1. 3) developed by Yuon and Trick [120], can be used to estimate the capacitance of the interconnect structures.... (1. 2)... (1. 3)The above case is the simple case but in practical case, at times, is not completely isolated from surrounding. The total parasitic capacitance of the line is not only increased by the fringing field effect, but also by capacitive coupling between the lines.

1. 2. 2 Interconnect Resistance

In present DSM CMOS technologies, copper has been adopted to replace aluminum as the primary interconnect material due to the lower resistivity of copper as compared to aluminum. Figure 1. 3: Cross-Sectional Area of Interconnect. The DC-resistance R_{dc} , for interconnect as shown in Figure 2. 9 and given by Eqn. (1. 4)...(1. 4) where ρ is the metal resistivity and $A = wh$ is the wire cross section area. The sheet resistance, $R_{sq} = \rho/h$, which gives the resistance per square of interconnect is normally tabulated for semiconductor processes. Eqn. (1. 4) is sufficient at low signal frequencies when the entire cross section of the wire carries the current. But, the current density starts to fall off exponentially into the conductor as signal frequency increases. This phenomenon is known as skin effect. The most of the current is now flowing through the "skin" of the conductor in this condition. The skin depth, δ , is the depth at which the current density has decreased by a factor e^{-1} of its value at the surface and is given by Eqn. (1. 5)...(1.

5) Where, f is the signal frequency and μ is the permeability. By making interconnects taller, the cross sectional area of the conductor grows, which helps to lower the resistance. For each new technology node, the wire Aspect Ratio ($AR = h/w$) has gradually changed from thin and wide to tall and narrow. In advanced processes, the top metal layer AR is typically close to 2. Copper has recently replaced aluminum as interconnect material in top metal layers to further reduce wire resistance. Since copper, unlike aluminum, diffuses into most dielectrics, must be encapsulated by suitable metal or dielectric barrier. For on-chip Copper interconnect, a thin and highly resistive barrier layer is built on three sides of interconnect to prevent Copper from diffusing into surrounding dielectric, as shown in Figure 1. 3. This barrier layer consumes part of the cross sectional area allocated to interconnect. The effective resistivity ρ_{eff} due to this barrier induced reduction in the cross sectional area. The resistivity of copper increases approximately linearly with temperature

1. 2. 3 Interconnect Inductance

As mentioned earlier, whenever a driving circuit forces a voltage and current signal onto a conductor, an electric and magnetic field is induced around it. The process of building up the current flow is not instantaneous but rather takes some finite amount of time. The unwillingness of the current to ramp up or down straightaway is called inductance ' L '. Inductance is only defined for current loops. Therefore, the inductance of a line is the self-inductance of the loop formed by the signal wire and its return. Any current injected into a system must somehow return to the source. Thus, when a current I is injected into a signal conductor, there must be a net current of $-I$ flowing in a

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return path. Current can return through the substrate or through nearby DC-paths. Some return current is in the form of non-negligible displacement current through interconnect capacitances. Since inductance has a long range effect, the return paths are not known beforehand. In general, current will always return through the path of least effective impedance. Therefore, low-speed current follows the path of least resistance, while high-speed current flows through the path of least inductance located as close to the signal line as possible. This high-frequency behavior is called the proximity effect. Total inductance is the sum of external inductance (the current flowing on the conductor surface), and internal inductance (due to current flowing inside the conductor). At very high frequencies, the current tends to crowd at the conductor surface due to the skin effect. Thus, as frequency increases, the total inductance falls asymptotically towards the external inductance value. One way to gain control over the wire behavior is to provide a dominant current return path close to the signal wire. Assume a signal loop A. The most basic definition of inductance originates from a fundamental relation between the voltage, V , and the current, I associated with the loop. A voltage drop is created when the current flow through the loop changes as from Eqn. (1. 6)....(1. 6) In cases when a conductor is completely surrounded by a homogeneous uniform dielectric, the capacitance, c , and inductance, l , per unit length are related by as Where, ϵ is the dielectric constant and μ is the permeability. For lossless lines, inductance can also be calculated from capacitance through Eqn. (1. 7), which describes the speed, v , at which an electromagnetic wave travels through a medium....(1. 7) Thus, the maximum effective velocity for

on-chip signals is around two times slower than in vacuum since $r = 3.9$ for SiO_2 , typically used as insulator. However, real wires are not lossless and a process stack typically includes insulators with different dielectric constants on adjacent levels. As compared with resistance and capacitance, the interconnect inductance is significantly more difficult to extract. One reason for this difficulty is due to the loop-based inductance definition as Eqn. (1.8). (1.8) Where, ϕ_{ij} is magnetic flux in loop i induced by current I_j in loop j . To form a loop, the current return paths need to be identified. The current distribution in a circuit, however, a priori depends on interconnect characteristics. The effect of inductance in wide global interconnects in top metal layers is more significant than that of local interconnects in lower metal layers. Since the wires in adjacent layers are generally orthogonal, adjacent layers can no longer be treated as a ground plane as in capacitance extraction. Another reason for the difficulty in inductance extraction is due to long range inductive coupling effects. One way to avoid determining a priori current return path is to use the concept of partial inductance. In determining the partial inductance, the flux area extends from conductor to infinity. The loop inductance of a closed loop can be uniquely determined by partial self-inductance of each segment of loop and partial mutual inductance between any pair of those segments. Partial inductance nonlinearly depends upon the interconnect length. This behavior is result of inductive coupling among different segments of the same line. For a loop formed by two closely placed parallel interconnects (where the length of the loop is more than ten times longer than the loop width), the loop inductance depends linearly on the length of the loop. The inductance of a wire not

forming a closed loop has no physical meaning. As an alternative to the PEEC model, a loop-based inductance model is preferred in well designed interconnect structures, such as shielded buses and clock distribution networks. In early design stages, a good assumption regarding the current return path is the nearby lower/ground networks, since these tracks are generally wide with low resistive impedance. Inductance is also a function of frequency due to the variation of the current distribution with frequency. In addition to the skin effect mentioned earlier, the current distribution inside a conductor also changes with frequency due to the proximity effect. If the current in these two wires flows in opposite directions, the currents concentrate towards each other; otherwise, the two currents shift away from each other. Both the skin effect and the proximity effect are essential due to same mechanism. The resistance of conductor also depends on neighbor line signal activities due to proximity effect at high frequencies. Another effect of frequency on the inductance is due to multi-path current redistribution. In an integrated circuit, there are many possible current return paths, e. g., the power/ground network, nearby signal lines, and the substrate. The distribution of the return current among these possible paths is determined by the impedance of the individual paths. At different frequencies, the relationship among the impedances of different paths will change, as well as the distribution of the return current. The return current is distributed in those paths so as to minimize the total impedance at a specific frequency.

1.3 INTERCONNECTS CHARACTERISTICS

Typical signal integrity effects include interconnect delay, crosstalk, transmission line effects, substrate coupling, power supply integrity, and

noise-on-delay effects. In the early days of VLSI design, these effects were negligible because of relative slow chip speed and low integration density. However, with the introduction of technology generations at about the 0.25 μ m scale and below, there are many significant changes in wiring and electrical characteristics. Interconnect started to be a dominating factor for chip performance and robustness. The characteristics affect the behavior of interconnects are delay, power dissipation and crosstalk

1. 3. 1 Delay

With decreasing feature sizes and increasing signal speeds. The problem of modeling gate delay becomes more difficult. As technology approaches the DSM region, the portions of delay contributed by gates reduced while the delay due to interconnects become dominant. This is because of interconnect lengths do not scale in proportion to the shrinking area of transistors that make up the gates. The on-chip inductance can play a significant role for determining the interconnect delay for long wide wires as the operating frequencies also increase with scaling. It is no longer true that a path delay is equal to the sum of all delays for long wide wires. However, wire delays can be taken into account in the path-delay fault model based on the physical layout, as interconnections are included in the paths.

Interconnect delay is a primary design criterion due to the close relationship to the speed of a circuit. Early interconnect design methodologies focused primarily on delay optimization. A typical data path in a synchronous digital circuit is shown in Figure 1. 4. In the case of zero clock skew, the minimum allowable clock period is as Eqn.(1. 9)...(1. 9)Where, t_{int} is the time required for the data to leave the initial register after the clock signal arrives, T_{int} is the

interconnect delay, $T_{logicmax}$ is the maximum logic gate delay, and T_{setup} is the required setup time of the receiving register. From (interconnect logical), by reducing T_{int} , the clock period can be decreased, increasing the overall clock frequency of the circuit. Figure 1. 4: Data Path in a Synchronous Digital System

Communication among these cores and on-chip memories generally requires multiple clock cycles. By reducing the interconnect delay, the speed of the system and computational efficiency of the system can be improved. The resistance and capacitance are distributed along the transmission line after the estimation of the total resistance and capacitance. If we consider the N segments in transmission line, Delay can be estimated as with Eqn. (1. 10)...

(1. 10) Fault free operation of a large circuit requires not only performing the logic function correctly but also propagation of correct logic signals along paths within a specified time limit. A delay fault causes excessive delay along a path. The total propagation delay falls out-side the specified limit is not in consideration. Delay faults have become more prevalent with decreasing feature sizes. There are different delay fault models as gate-delay fault and the transition fault models, a delay fault occurs when the time interval taken for a transmission from the gate input into its output exceeds its specified range. It should be noted that simulation transmission at inputs of a gate may change the gate delay significantly due to activation of multiple charge/discharge paths. The other model is path-delay fault. Which consider the cumulative propagation delay along the path therefore, the path delay fault model is more practical for testing then gate-delay fault. In most practical cases the number of paths in circuit makes it impossible to enumerate all path-delay faults for the

purpose of test generator fault simulation. Delay can be calculated by using the Eqn. (1. 11).... (1. 9)Where; The difference in propagation delays of logic elements is the major contributor to glitches in asynchronous circuits as a result of race conditions. The principle of logical effort utilizes propagation delays to compare designs implementing the same logical statement.

Propagation delay increases with operating temperature, marginal supply voltage as well as an increased output load capacitance. The latter is the largest contributor for the increase of propagation delay. If the output of a logic gate is connected to a long trace or used to drive many other gates i. e. high fan-out the propagation delay increases substantially. The delay effects are depends on the transitions in the lines depicted as Table 1. 1. The worst case delays are class 4, 5 and 6 in Table 1. 1. Table 1. 1 Delay of line K in three lines

Transition	Delay Of Line K	Cross talk Class (CC)
01		
12		
1+λ3		
1+2λ4		

’ ’ ’ ’

’ ’ ’

01

’

12

’ ’ ’

1+λ3

’ ’ ’ ’

’

1+2λ4

’ ’ ’

$1+3\lambda 5$

,

$1+4\lambda 6$ for transition from 0 to 1, for transition from 1 to 0 and for no transition. Most integrated circuit wires are designed in a way that makes the resistive attenuation very large. As a result, the RC term dominates and signal propagation. The wires can be described by simplified RC-chains. This is the classical view of an integrated circuit wire, characterized by large delays (much larger than velocity-of-light delays). A typical solution to improve the latency of RC-wires is to split interconnect into an optimum number of equal-length segments, and to insert an inverter (repeater) between each such segment. By inserting an optimum number of repeaters, one can make the total wire delay proportional to length d .

1. 3. 2 Crosstalk

When a signal travels down a transmission line, the electric and magnetic field energy can couple to other nearby conductors. This crosstalk coupling occurs directly through the mutual capacitance and mutual inductance between wires, and indirectly through the impedance of shared return paths. Crosstalk acts as a noise source, which reduces noise margins and can cause signal integrity problems. The capacitive crosstalk through the Miller-effect on inter-wire capacitances considered in on chip buses. The inductive coupling effects are not negligible and will become an issue as switching frequencies increase to multi-GHz rates. Crosstalk effects can be separated to two categories as crosstalk glitches and crosstalk delays. The substrate

coupling is particularly harmful in mixed signal. ICs where the low resistive silicon substrate can be modelled as a resistive and capacitive network and the noise can spread globally through this network. Substrate crosstalk is closely related to the chip package and the power/ground distribution network. A good power and ground distribution design is most important for reducing substrate crosstalk. Besides, signals can affect one another via a shared power supply or ground. Crosstalk delay is a signal delay that is provoked by the same coupling effects among interconnect lines, but it may be produced even if line driver are balanced but have large loads because crosstalk causes a delay in addition to thermal gate and interconnect delay, it is difficult to estimate the true circuit delay, which may lead to severe signal delay problem. Conventional delay fault analysis may be invalid if these effects are not taken into consideration based on the physical layout. VDSM technology contains the new reliability and testing challenges, due to the ICs reduced internal nodes capacitance, power supply and noise margins. As in VSDM wires are more close or lower inter-wire spacing and long so coupling capacitance and resistance of interconnect wires will be higher due to tall and thin conductors as compared to the previous technology. When these conductors are placed together, it forms parallel plate capacitors, known as inter-wire capacitance or coupling capacitance (C_p) this coupling capacitance cause crosstalk effect involves more and more become main cause of noise and delay and uncertainty in the bus. This is case by which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel. Crosstalk is usually caused by undesired capacitive, inductive, or conductive coupling from one circuit,

part of a circuit, or channel, to another. Crosstalk is the capacitive and inductive coupling of signals from one signal line to another. As system performance and board densities increase causes the problem of crosstalk. Crosstalk noise can cause false switching by crossing the threshold regions of receivers on the passive line. Crosstalk coupling generates two types of effects: forward cross-talk and reverse cross-talk.

1. 3. 2. 1 Forward crosstalk

Forward crosstalk is defined as the current coupled onto a passive line away from the active line driver as shown in Figure 1. 5. Forward crosstalk current is the result of capacitive coupled current (I_C) minus the inductively coupled current (I_L) i. e. $I_C - I_L$. This is due to the inductively coupled current traveling in the direction of the end of the passive line away from the active line driver (point D in Figure 1. 1). Forward crosstalk coupling occurs during the edge transitions on the active line and in opposite polarity. The pulse amplitude is a result of the difference in capacitive and inductive coupling. Due to the short duration and small amplitude of forward crosstalk, the reflections of reverse crosstalk often hide this small pulse. Figure 1. 5:
Forward Crosstalk

1. 3. 2. 2 Reverse crosstalk

Reverse crosstalk is defined as the current coupled onto a passive line toward the active line driver as shown in Figure 1. 6. Reverse crosstalk current is the result of capacitive coupled current (I_C) plus the inductively coupled current (I_L) i. e. $I_C + I_L$. This is due to the inductive coupling resulting in a transformer action. Reverse crosstalk is directly proportional to

line length and velocity of propagation on the line. Reverse crosstalk increases linearly with distance up to a certain length. This length is the distance that the signal can travel during its rise or fall time. Figure 1. 6: Reverse Crosstalk As illustrated in Figure 1. 6, reverse crosstalk coupling starts at point C simultaneously with the beginning of the transition at point A. This coupling continues for the duration that active line is switching. As the signal propagates down the active line to point B, the signal is coupled onto the passive line and toward point C. The reverse crosstalk then requires another flight time to reach point C. This makes the total reverse crosstalk waveform on passive line twice the distance of the active line. Depending on the termination of passive line, a reflection can be generated from reverse crosstalk, and this reflection will propagate to D depending upon amplitude and duration, back to C.

1. 3. 2. 3 Crosstalk mechanisms

Consider the two symmetrical and coupled transmission lines (A and B) in Figure 1. 7. Line A (aggressor) is driven at the near-end and terminated in its characteristic impedance, Z_0 , at the far-end. Line B (victim), is terminated in its characteristic impedance at both ends. When a voltage step is driven onto line A, it starts to move from its near end, P1, to its far end, P2. At each point along the line, a fraction of the signal is coupled from the aggressor to the victim line and starts to move towards both victim ends, P3 and P4. The mutual capacitance couples the time derivative of voltage as Eqn. (1. 10).

Figure 1. 7: Forward and Reverse Crosstalk Waves Created by Capacitive and Inductive Coupling...(1. 10) Where, k_{cx} is the capacitive coupling coefficient including the mutual capacitance between the wires, c_m , and the wire

capacitance to ground, c_0 , per unit length. Thus, a positive time derivative of voltage on Line A induces a positive forward traveling wave, and a positive reverse traveling wave on Line B at the point of capacitive coupling.

Similarly, mutual inductance couples the spatial derivative of voltage as Eqn.

(1. 11)....(1. 11)Where, k_{lx} is the inductive coupling coefficient including the mutual inductance between the wires, m , and the wire self inductance, l , per

unit length. The relation between spatial and time derivatives of waves is

given by Eqn. (1. 12)....(1. 12)Where, v is the propagation velocity and V_f , V_r is

a forward and reverse travelling wave, respectively. Therefore, a positive

spatial derivative of voltage on Line A induces a negative forward travelling

wave, and a positive reverse travelling wave on Line B at the point of

inductive coupling. A total forward wave (far-end crosstalk) and total reverse

wave (near-end crosstalk) is obtained by superposition of the forward and

reverse waves induced by capacitive and inductive coupling. It is shown that

the total forward coupling coefficient, k_{fx} , and total reverse coupling

coefficient, k_{rx} , is given by Eqn. (1. 13)....(1. 13)As an edge with rise time t_r

propagates towards the far-end on the aggressor line, it continuously

couples energy into the victim wire. The forward (far-end) crosstalk wave

moves side-by-side with the edge on the aggressor line and reaches its end

after a line delay, t_d , where it is absorbed in the termination impedance

during a time of t_r . The reverse (near-end) crosstalk wave starts at the

aggressor edge and moves towards the near-end of the victim line during a

total time of $2t_d$ (round trip from P3 to P4 and back again). For interconnects

surrounded by a homogeneous dielectric, $k_{cx} = k_{lx}$, which cancels the far-

end crosstalk, since $k_{fx} = 0$. However, if the near-end has an unmatched

termination, reflections of near-end crosstalk can still become a far-end problem. There is always both near- and far end crosstalk in a non-homogeneous environment. Crosstalk causes variations in the transmission line parameters, which in turn affects the effective characteristic impedance and signal propagation delay. The simplified circuit model of two coupled transmission lines (A and B) in Figure 1. 7, can be used to derive first order equations describing the principle of data-dependent inductance and capacitance. Kirchoffs voltage law gives Eqn. (1. 14)....(1. 14)Similarly, Kirchoffs current law yields Eqn. (1. 15)....(1. 15)For “ odd-mode” propagation, the signal injected into line A transitions in a direction opposite to the signal injected into line B making $I_A = -I_B$ and $V_{A2} = -V_{B2}$. Using I_A and V_{A2} values in Eqn. (1. 14) and Eqn. (1. 15) obtained Eqn.(1. 16)....(1. 16)Thus, the effective odd-mode inductance and capacitance on each line is $L_{odd} = (L - M)$ and $C_{odd} = (C_0 + 2C_m)$, respectively. Similarly, for “ even-mode” propagation, the signal injected into line A transitions in the same direction as the signal injected into line B, which makes $I_A = I_B$ and $V_{A2} = V_{B2}$. Using I_A and V_{A2} values in Eqn. (1. 14) and Eqn. (1. 15) obtained Eqn. (1. 17)....(1. 17)Thus, the effective even-mode inductance and capacitance on each line is $L_{even} = (L + M)$ and $C_{even} = C_0$, respectively. This results in not only data-dependent characteristic impedance, Z_0 , but also variations in signal velocity. Table 1. 2 summarizes the data-dependent characteristic impedance and propagation velocity trends for two coupled transmission lines. Table 1. 2: Trends for data-dependent characteristic impedance, Z_0 , and propagation velocity, for two coupled transmission lines. Data Pattern Z_0 voror Since the shields and ground return plane minimize the

mutual capacitance between the wires, the effective capacitance on each signal line should be approximately independent of data-pattern. However, long-range inductive coupling remains and dominates over any remaining capacitive coupling. Therefore, the velocity should increase for an odd-mode switching pattern and decrease for an even-mode pattern, according to the propagation velocity trends in Table 1. 2. Thus, any impact of dominating inductive coupling should result in delay variations which have a sign opposite to what would be obtained through classical Miller-effect, triggered by dominating capacitive coupling. The crosstalk-induced delay variations through inductive coupling can cause timing issues as on-chip global buses become longer and switching frequencies reach multi-GHz rates. Either capacitive or inductive coupling dominates and the two have opposite sign. The coupling between the groups of the three wires is classified into five Types depending upon the nature of transitions of signals in the wires as per Table -1. 3. These are Type-0, Type-1, Type-2, Type-3 and Type-4. The Type-0 coupling occurs when all of the 3-bit wires are in the same state transition. A transition from 000 to 111 (i. e. $\uparrow \uparrow \uparrow$) causes a Type-0 coupling. For Type-0, coupling capacitance is zero. Type-1 coupling occurs when there is a transition in one or the two wires (including the centre wire) and the third wire remains quite. There are eight possibilities by which Type-1 condition occurs. The coupling capacitance in this case is C_c . A Type-2 coupling occurs when the centre wire is in the opposite state transition with one of its adjacent wires while the other wires undergo the same state transition as the centre wire i. e. 100 to 011. Ten conditions are possible for Type-2 coupling. The coupling capacitance is $2 \cdot C_c$ in this case. A Type-3 coupling occurs

when the centre wire undergoes the opposite state transition with one of the two wires while the other wires are quiet i. e. 010 to 001. Coupling capacitance in the case of Type-3 coupling is $3 \cdot C_c$ and there are four possibilities that causes Type-3 coupling. For a Type-4 coupling, all three wire transitions in the opposite states with respect to each other. Two conditions cause Type-4 coupling with a coupling capacitance effect of $4 \cdot C_c$. All the five Types of couplings are shown in Table-1. 3. Table 1. 3: Crosstalk Types of a 3-Bit Bus When Considering RC Effects [2]

Type-0	Type-1	Type-2	Type-3	Type-4
↑	↑	↑	↑	↑
↓	↓	↓	↓	↓
-	-	-	-	-

↑: switch from " 0" to" 1", ◆": switch from " 1" to " 0", - : no transition
The crosstalk highly depends upon the transitions of the signal in the wires.

1. 3. 3 Power Consumption in Interconnects

There are mainly two types of power consumption exist for digital CMOS. The first, the dynamic power component, may be thought of as useful because it establishes information by charging and discharging signal lines; the second type, consisting of short-circuit and static power components, is waste and comes from short-circuit and leakage currents that flow directly from the power supply to ground.

1. 3. 3. 1 Dynamic power dissipation

The dynamic power dissipation is the power required for the circuit to perform its anticipated tasks. In other words, it is the power needed for charging and discharging all nodes in a CMOS circuit. This power is only consumed when the circuit input signals change. In CMOS circuits, the dynamic power dominates the total power dissipation. Such characteristic is

greatly affected by current processes or the deep sub-micron processes (DSM), for which the ratio of leakage power to dynamic power is increasing. Power Dissipation due to higher clock frequencies and on-chip integration levels, has significantly increased. The dynamic power due to the interconnect capacitance can be greater than 50% of the total dynamic power. Furthermore, the repeaters and pipeline registers inserted in interconnect introduce additional dynamic, leakage, and short-circuit power. High power dissipation increases packaging cost due to heating problems and shortens the battery life in portable applications. Power dissipation, therefore, is another important criterion in interconnect design. For the inverter circuit, conduction and non-conduction of NMOS and PMOS creating a direct path from the output load to ground and allowing the output load to discharge. If C_L represents the total capacitance charged per cycle, then the dynamic power dissipation is as Eqn. (1. 18)....(1. 18)Where, V_{dd} is the supply voltage level, f is the frequency of operation, and α is the switching activity of the capacitive node C_L on each clock cycle. Even though the above analysis is for a simple inverter, a similar approach can be followed to evaluate the dynamic power dissipation for a circuit with n nodes; in such a case, the total dynamic power dissipation is evaluated as Eqn. (1. 19)....(1. 19)Where, α_i is the switching activity of node i with capacitance C_i . If C_{eff} represents the average switching capacitance per cycle, then the corresponding power dissipation equation represents the average dynamic power dissipation as Eqn. (1. 20)....(1. 20)Even though, the device dimensions and the device capacitances are scaled down with newer technologies, but the total capacitance per chip increases. In addition, two of

the main requirements of current applications are speed and real-time operation. As such, the frequency of operation is meant to increase drastically in the microprocessor and in general area. The supply voltage is not scaled at the same rate as the device scaling for a specific technology. From these facts, the relative power is increasing with respect to that of predecessor technologies. These equations are vital in investigating new techniques targeting lower power dissipation of CMOS chips and are important for addressing the dynamic power dissipation that is the dominant factor in the total power dissipation of CMOS circuits.

1. 3. 3. 2 Short circuit power dissipation

The dynamic power dissipation equation is derived usually by assuming that the inputs have zero rise and fall time. But in reality, such assumption is not valid, and input signals have nonzero rise and fall times. Hence, a direct current path exists between V_{dd} and GND for a short period of time during input switching, in which case the PMOS and the NMOS devices are simultaneously conducting. This power component is consumed without attributing to the circuit behavior. The short circuit power dissipation can be stated as Eqn. (1. 21)....(1. 21) where I_{sc} is the current leaking when both transistors are on during switching. For a system with n gates, the total short circuit power dissipation can be expressed as Eqn. (1. 22)....(1. 22)

1. 3. 3. 3 Static power dissipation

The static power consumption of static CMOS circuits is assumed to be zero, as the PMOS and the NMOS devices are never on simultaneously in steady-state operation. But in reality, the drain current through the CMOS transistor

does not drop to zero. Unfortunately, there is always a leakage current which is primarily determined by the fabrication technology. The contribution of the static power dissipation to the overall power dissipation is in general very small and can be ignored. However, with the current technologies, for which reductions in the device threshold voltage are employed for achieving better performance, the percentage of the static power dissipation from the total power has increased. A variety of leakage currents are steadily flowing through various parts of the transistor, including a sub threshold current through the channel. Those currents are small, but they become important in low-power applications. Not only do many circuits need to operate under very low current drains, but sub threshold currents are also getting relatively larger as transistor sizes shrink.

1. 3. 3. 4 Power consumption considerations

The dependence of the power consumption on many parameters allows the VLSI designer to have a large number of techniques available to reduce the power dissipation. The following parameters should be considered when designing for low power viz. power-supply voltage, device-threshold voltage, physical node capacitance, and switching frequency. Unfortunately, a speed penalty is paid for supply voltage reduction, with delays drastically increasing as V_{dd} approaches the threshold voltage V_t of the devices. This tends to limit the useful range of V_{dd} to a minimum of about 2 to 3 V_t . Effectively, speed optimization techniques are applied and then the supply voltage is scaled which bring the design back to its original timing but with a lower power requirement Benini et al., 2001. Dynamic power component is the power expended while charging and discharging of capacitive nodes.

This physical capacitance is attributed to the transistor parasitic capacitance and the interconnect capacitance. Reducing these capacitive nodes could result in substantial power reductions across the whole system. So, minimizing capacitances offers another option for minimizing power consumption. The capacitance load of a circuit is made of two components: intrinsic and extrinsic. Intrinsic capacitance refers to internal parasitic capacitances of the circuit, and they consist of drain and source to substrate and overlap capacitances. The extrinsic capacitances are the parasitic capacitances of the fan-out, driven by the circuit and the routing capacitances resulting from the routing between the circuit and its fan-out gates. Accordingly, capacitances can be kept at a minimum by using less logic, smaller devices, and fewer and shorter interconnects. Power consuming transitions should be avoided whenever possible. Dynamic power dissipation is only consumed when there is switching activity at some nodes in a CMOS circuit. For example, a chip may contain an enormous amount of capacitive nodes, but if there is no switching in the circuit, then no dynamic power will be consumed. The switching frequency determines how often the switching occurs. Normally, f increases with technology scaling, The node switching activity per cycle, α has two components: useful data switching activity (UDSA) and redundant spurious switching activity (RSSA). The UDSA can be interpreted as the probability that a useful power consuming transition will occur during a single data period. The calculation of this term is difficult because it depends on the input switching activity, logic function implemented, and the spatial and temporal correlations among the circuit inputs. Glitching refers to spurious and unwanted transitions occur before a

node settles down to its final steady-state value that occurs due to partially resolved functions as discussed earlier. Glitching often arises when paths with unbalanced propagation delays converge at the same point in the circuit. Because, Glitching can cause a node to make several power-consuming transitions, it should be avoided whenever possible.

1.3.4 Noise

With interconnect scaling, coupling capacitance between and among interconnects dominates the ground capacitance. Furthermore, inductive coupling has to be considered due to increasing signal frequencies, making coupling noise more significant and complicated. Interconnect coupling induced noise can be classified into two categories voltage level noise and delay uncertainty interconnect coupling as shown in Figure 1. 8. Noise may cause a malfunction in circuit if noise level is greater than a certain threshold. In addition to coupling effects, delay uncertainty can also be caused by other factors, such as process variations on both interconnects and the inserted repeaters or pipeline registers, temperature variations, and power/ground noise. Delay uncertainty is both spatially dependent due to process variations and temporally dependent due to coupling, temperature variations, and power/ground noise. Timing margins are assigned to manage this delay uncertainty, thereby increasing the clock period and reducing the overall performance of the circuits. When delay uncertainty exceeds these margins, setup or hold violations may occur, reducing the yield. Figure-1. 8: Form of Noise in Three Line Interconnect

1. 4 INTERCONNECT MODELS

Interconnect modeling is critical in both circuit design and verification processes. An efficient and accurate interconnect model can significantly enhance these processes. In later Subsections describe models of single interconnect and coupled interconnects.

1. 4. 1 Single Interconnect

The single interconnect model is the basis for many interconnect network simulation tools. Various on-chip interconnect models have been presented over the past several decades, from lumped C/RC/RLC models to distributed transmission lines. A tradeoff between efficiency and accuracy is required in selecting the appropriate model.

1. 4. 1. 1 Lumped models

The circuit behavior is typically dominated by the capacitance and effective resistance of the gates for local interconnects with a length of tens of micrometers and below. Modeling of interconnect as a lumped capacitance or lumped RC structure is generally accurate enough. Commonly used lumped models include L, T, and π shaped structures, as depicted in Figure 1. 9. Figure 1. 9: Lumped Interconnect Model Distributed models for long intermediate and global interconnects, the signal propagation delay along interconnect is larger than the gate delay. In this case, the distributed characteristics of interconnect should be considered. Distributed interconnect can be characterized by the Telegrapher's equations in transmission line theory as Eqn. (1. 23)....(1. 23) Where, R, L, and C are the interconnect impedance parameters per unit length, x is the distance along

interconnect, and s is the complex frequency. The conductance between the signal line and ground can typically be ignored in on-chip structures. If the interconnect is non-uniform, these parameters are a function of x . If frequency dependent effects need to be considered, these interconnect parameters are also a function of s . Besides the difficulties in inductance extraction, including inductance in the model also makes circuit analysis more complicated due to inductance induced signal reflection, ringing, and coupling effects. To characterize the condition when on-chip inductance is considered shown as Eqn. (1. 24)....(1. 24) Where, t_r is the signal transition time and l is the interconnect length. Transmission line models are based on transverse electro-magnetic (TEM) mode or quasi- TEM mode wave propagation. The TEM or quasi-TEM mode assumption is valid when line cross sectional dimension is much smaller than the wavelength. This requirement can be generally satisfied in on-chip structures. When using a transmission line model, both the resistance and the inductance should be extracted from the loop formed by the signal line and the ground return path. Since the resistance of ground return path is generally much smaller than that of signal line, the resistance of ground can be ignored.

1. 4. 1. 2 Lumped representation of distributed interconnects

A transient time domain simulation of a transmission line can be grouped into two categories as impulse response convolution and lumped equivalent circuits. In the first method, the transmission line is initially analyzed in the frequency domain. Next, a time domain impulse response (called a Green's function) is obtained based on the frequency domain solution. Finally, the time domain solution is determined by convolving the Green's function with

the voltages at the line ports. The second method is to partition the transmission line into a number of segments and model each segment as a lumped structure. Additional segments provide more accurate results, but consume more computational resources. The key issue in this method is to determine the appropriate number of segments. Using lumped models to represent a distributed transmission line introduces inaccuracy when evaluating circuits that operate at high frequencies. The highest frequency of interest, therefore, should be determined in order to evaluate the maximum error induced by using lumped models. The frequency domain representation of a normalized saturated ramp signal with rise time t_r is as Equation-1. 25...

(1. 25) After partitioning a distributed line into lumped segments, frequency dependent effects can be modeled in each segment by a ladder structure of frequency independent lumped RL elements, as shown in Figure 1. 10. Additional ladder stages provide higher accuracy when operating at high frequencies. The value of the circuit elements can be obtained by matching the impedance of the model to the extracted impedance at different frequencies. Figure 1. 10: Modeling Frequency Dependent Impedance with Lumped Element

Modeling parallel coupled interconnects draws special attention in the circuit design process due to the commonly used bus structure. A general solution for coupled multi-conductor systems is composed of two steps, decoupling the systems into independent interconnects, followed by applying single line models to each of these interconnects.

1.5 TECHNIQUES FOR HANDLING INTERCONNECT ISSUES

In general, power minimization targets maximum instantaneous power or average power. Optimizations can be achieved by facing the power problem from different perspectives as design and technology. Enhanced design capabilities mostly impact switching and short-circuit power technology improvements. From a design perspective, circuit designers can choose from a number of options to reduce the power dissipation ranging from the highest levels of abstraction (architecture level) to the lowest levels of abstraction (physical or technology level). In each level of abstraction, there exist a number of techniques that can be employed to effectively reduce the power dissipation of CMOS circuits, all of which can be obtained from the power dissipation equations mentioned in the previous sections. As each technique has its own figure of merit, it usually affects one or more aspect of the system being optimized. As such, attempts are always being made to find a compromise that can effectively present a fair and reasonable solution among conflicting objectives like power dissipation and performance, where improving one generally means degrading the other. Actually, addressing the power problem from the very early stages of design development offers enhanced opportunities to obtain significant reductions of the power budget and to avoid costly redesign steps. The stages during the design involve the system, architectural, logic, circuit, and physical levels.