Low noise amplifier and design essay

The largest signal can be received by a receiver establishes the upper power level limit of what can be handled by the system while preserving voice or data quality. The dynamic range of the receiver, the difference between the largest possible received signal and the smallest possible received signal, defines the quality of the receiver chain. The LANA function, play an Important role in the receiver designs. Its mall function Is to amplify extremely low signals without adding noise, thus preserving the required Signal-to-Noels Ratio (SIN) of the system at extremely owe power levels.

Additionally, for large signal levels, the LANA amplifies the received signal without introducing any distortions, which eliminates channel interference. ; An LANA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. ; Although Gain, Noise Figure, Stability, Linearity and input and output match are all equally important, they are interdependent and do not always work in each other’s favor. Carefully selecting a transistor and understanding parameter trade-offs can meet most of these conditions. ; Low noise figure and good Input match Is really simultaneously obtained without using feedback arrangements. ; unconditional stability will always require a certain gain reduction because of either shunt or series resistive loading of the collector. High PIP requires higher current draw, although the lowest possible noise figure is usually achieved al lower current levels. Envelope termination technique can be used to improve PIP performance while operating LANA at low current levels. Additional improvement of PIP can also be achieved by proper power output

matching (Ida compression point match or Pled match). The Pl db match, being different from conjugate match, reduces the gain although improving PIP performance. ; Transistor selection is the first and most Important step In an LANA design. The designer should carefully review the transistor selection, keeping the most Important LANA design trade-offs In mind.

The transistor should exhibit high gain, have a low noise figure, and offer high PIP performance at the lowest possible current consumption, while preserving relatively Examination of a data sheet is a good starting point in a transistor evaluation for LANA design. The transistor’s S-parameters should be published at different collector/emitter voltages and different current levels for frequencies ranging from low to high values. The data sheet should also contain noise parameters, which are essential for low noise design. Spice models for the transistor and its package are also useful for PIP and Pled simulations.

The designer should first look at the main design parameters as: Noise, Gain, and PIP, and decide what Vice and LLC levels will produce optimal reference. The forward transducer power gain represents the gain from transistor itself with its input and output presented with 50 Q impedance. The manufacturer of the transistor at multiple frequencies and different Vice and current levels provides the SIS values. Additional gain can be obtained from source and load matching circuits. Maximum Stable Gain and Maximum Power Gain (Gamma) are good indicators of additional obtainable gain from the LANA circuit.

LANA linearity is another important parameter. A figure of merit for linearity is PIP. A two-tone test is used for derivation of PIP. As a rule of thumb for bipolar Junction transistors (BIT), the Output-PIP can be estimated from the following formula: Loop[debt-n] = 10 log (vectors] * Cacti] * 5) ; RFC performance of the LANA depends by many variables as: – Frequency – DC Biasing and Power Dissipation – Stability – Input and Output Matching – Layout and Grounding – ME Shielding – Supply decoupling – Temperature 1. DC Biasing (BSTJ) represent the first step in LANA design. The chosen DC bias circuit should exhibit stable thermal performance and reduce the influence of wife spread. ; The resistive feedback arrangement is the simplest form of DC biasing that fulfills al the major requirements. ; Two bias feedback arrangements are possible: one with a combination of Arc and Rub and a second one with simple Re and Ce combination. The operation of the Arc and Rub is simple: Arc and Rub will establish a biasing point. If the device current increases, the voltage drop across Arc increases, reducing the voltage seen by the base, thereby providing feedback.

Because the operation class of the LANA is going to be Class-A (constant current draw for dynamic range of power levels), a stable biasing point over different temperatures is required. For different lot resource matching, which is crucial for noise performance, the feedback network should be decoupled with an inductor (making biasing invisible at RFC band of operation). Another possible bias feedback can be realized with emitter resistor and capacitor. Ce should be selected carefully, because Re will also have a direct effect on RFC gain of LANA.

Ce should present a short at frequency of operation to limit its influence on gain and noise performance of the circuit. Other biasing methods are suitable for Class-A networks. These are usually closed feedback arrangements with dynamic bias control provided by active components. Although suitable for LANA application, these active feedback bias networks increase complexity of the LANA network, introduce additional components and increase the real-estate area of the solution. 2. Stability Design should be the next step in LANA design. Unconditional stability of the circuit is the goal of the LANA designer. ; Unconditional stability means that with any load present to the input or output of the device, the circuit will not become unstable – will not oscillate. Instabilities are primarily caused by three phenomena: internal feedback of the transistor, external feedback around he transistor caused by external circuit, or excess gain at frequencies outside of the band of operation. ; S-parameters provided by manufacturer of the transistor will aid in stability analysis: numerical and graphical. Numerical analysis consists of calculating a term called Roulette Stability Factor (Cofactor). ; When K-factor is greater than unity, the circuit will be unconditionally stable for any combinations of source and load impedance. ; When K-factor is less than unity, the circuit is potentially unstable and oscillation may occur with a certain combination of source and lord load impedance present to he transistor. The K-factor represents a quick check for stability at given biasing condition.

A sweep of the K-factor over frequency for a given biasing point should be performed to ensure unconditional stability outside of the band of operation. The designer’s goal is to design an LANA circuit that is unconditionally stable

for the complete range of frequencies where the device has a substantial gain. An LANA designer can use at least five methods for circuit stabilization. ; The first one consists of resistive loading of the input. This method, although capable of improving the debility of the circuit, also degrades the noise of the LANA and is almost never used. Output resistive loading is preferred method of circuit stabilization. This method should be carefully used because it effects are lower gain and lower Pled point (thus PIP point). ; The third method uses collector to base resistor-inductor-capacitor (RL) feedback to lower the gain at the lower frequencies and hence improve the stability of the circuit. ; The fourth method consists of filter matching, usually used at the output of the transistor, to decrease the gain at a specific narrow bandwidth frequency. This band of operation.

Short circuit quarter wave lines designed for problematic frequencies, or simple capacitors with the same resonant frequency as the frequency of oscillation (or excessive gain) can be used to stabilize the circuit. ; The final stabilization method can be realized with a simple emitter feedback inductor. A small inductor can make the circuit more stable at higher frequencies. But if the source inductance is increased, the K-factor at higher frequencies eventually falls bellow 1 . This effect limits the amount of source inductance that can safely be used. To get the best LANA stability performances have to accommodate the full range of expected variations in operating parameters as: o Component package parasitic o Component values o Temperature o Supply voltage ; Most common causes for LANA instability are: o Insufficient RFC decoupling between supply lines of the amplifier bias. O Parasitic inductance in AND connections. O Excess in-band and/or out-of-band Gain. O

Electro-Magnetic coupling and Feedback. ; Always check stability of your LANA well beyond band-of-interest checking for both, small-signal stability and for large-signal stability. Use stability circles on Smith Chart (for both, source and load) to verify legitimacy of chosen Zinc and Gout impedances. 3. Noise Matching and Input Return Loss (RL) The next step in LANA design consists of Noise Match and Input Return Loss (RL). ; RL defines how well the circuit is matched to 50 Q matching of the source. ; A typical approach in LANA design is to develop an input matching circuit that terminates the transistor with conjugate of Gamma optimum (rope), which represents the terminating impedance of the transistor for the best noise match. In many cases, this means that the input return loss of the LANA will be sacrificed.

The optimal RL can be achieved only when the input-matching network terminates the device with a conjugate of SSL 1, which in many cases is different from the conjugate of rope. ; In 1928 H. Iniquity showed that the noise from any impedance is determined by its resistive component. Consequently, if an ideal lossless element is used to provide feedback, than the minimum noise measure is unaffected. ; An emitter (or source) inductor feedback can rotate SSI closer to rope, which can help obtaining close to minimum Noise Figure and respectable RL simultaneously.

The additional series inductance provides lossless negative series feedback and also reduce the overall available gain of the network and can be used in balancing trade- offs between the gain, lip and stability in LANA design. Have to mention that this inductive degeneration does not seriously impact Noise Figure performance, as resistive degeneration does. At high frequencies this inductance will be achieved with small strip lines (stubs) connected directly

to the emitters of the transistor. The inductive reactant of the stubs is usually no greater than 10 Q and the line

To design an LANA for minimum Noise Figure, determine (experimentally or from the data sheet) the source resistance and bias point that produce the minimum Noise Figure for that device. ; Then force the actual source impedance to " look like" that optimum value with all stability considerations still applying. If the Roller stability factor (K) is calculated to be less than 1 (K is defined as a figure of merit for LANA stability), then you must be careful in choosing the source and load-reflection coefficients. A typical method used in designing input matching network is to display noise irises and gain/loss circles of the input network on the same Smith chart. This provides a visual tool in establishing an input matching network for the best Input Return Loss and noise trade off. Using Noise Figure from Datasets Generally for microwave transistors following a dataset the minimum Noise Figure (Fin) at higher frequencies is based on measurements, while the Fins at lower frequencies are extrapolated.

Fin represents the true minimum Noise Figure of the device when the device is presented with an impedance matching network that transforms the source impedance, typically 500, to an impedance represented by the reflection coefficient rope. The designer must develop a matching network that will present rope to the device with minimal associated circuit losses. To accomplish this have to minimize the number of components needed on the LANA input. The Noise Figure of the completed amplifier is equal to the Noise Figure of the device plus the losses of the matching network preceding the device.

The Noise Figure of the device is equal to Fin only when the device is presented with rope. If the reflection coefficient of the matching network is other than rope, then he Noise Figure of the device will be greater than Fin The losses of the matching networks are non-zero and they will also add to the noise figure of the device creating a higher amplifier noise figure. The losses of the matching networks are related to the Q of the components and associated printed circuit board loss. rope is typically fairly low at higher frequencies and increases as frequency is lowered.

For FEET devices larger gate width devices will typically have a lower rope as compared to narrower gate width devices. 500 is required for the device to produce Fin. At VHF frequencies and even lower L Band frequencies, the required impedance can be in the vicinity of several thousand ohms. Matching to such high impedance requires very hi-Q components in order to minimize circuit losses. 4. Output Matching The last step in LANA design involves output matching of the transistor. An additional resistor, either in series or parallel, has been placed on the collector of the transistor for circuit stabilization.

Conjugate matching has been exclusively used for narrow band LANA design to maximize the gain out of the circuit. With additional PIP requirement forced on the LANA, the trade-off between PIP and main must be considered. Linearity matching is widely known by high-power amplifier designers. The so-called load pulling is used to establish PIP and gain impedance contours. The load pulling can be realized by using the non-linear Spice model of the transistor with simulation software. Harmonic balance can be used for establishing two-tone environment.

The load pulling method sweeps impedance of the whole Smith chart and plots contours of the constant gain and PIP numbers. The optimal gain impedance does not match the optimal PIP point, which means that the design will have to be realized by means f a trade off. Typically, the designer should design the LANA circuit at the point where the gain does not degrade as much, and the PIP is still respectable. If one were to draw a line between the optimal gain and PIP impedance points, every point on that straight line will represent a good area of trade-off, with the ends representing the two optimal points.

The rule of thumb for Ida gain compression point (Pled) and PIP is: PIP = Bid +10 [darn] That means that by knowing the gain compression point (Pled), can estimates the PIP levels. ; The Dobb rule can further be improved with appropriate bypassing of the ease and the collector. As previously indicated, the lip is established by injecting two equal-in-magnitude signals with small frequency offset (S) into an active circuit. As the active circuit approaches non-linear region, close to Pled, the two carriers will generate distortion products, both in and out of band.

In example below we have two signals, with output levels Pout and frequencies Fl and IF. Loop[debt-n] = pout[debt-n] + IM[db] / 2 Where IM [db] is the difference in amplitude between one of the two equal amplitude test tones, present at the amplifier output, and the level of the highest rd-order distortion product. ; For every db increase in input power, the third order products (MIM) will increase db. ; For every db increase in input power, the second order products (MIM) will increase db.

Plotting third order products versus input power predicts a 3: 1 response which Second and Third-order Distortion Slopes Ida Gain Compression Point (Pled) The relation between Input-PIP (IPP) and Output-PIP (Loop) is defined as: lip[db] = Loop[debt-n] – Gate[db] The low frequency MIM products (IF-IF), can modulate the base-emitter and collector- emitter LANA supply voltages. To improve the linearity the fluctuation of the base and the collector shall be stabilized with low impedance at so called video frequencies or baseman frequencies (between DC and usually up to mash). The designer should exhibit caution during bypassing design. A poor selection of the by-pass capacitors could also degrade PIP performance. ; As a rule of thumb, the impedance of bypassing circuit should be lower than 25% of the input impedance of the transistor at particular frequency spacing. ; Although preserving the gain performance of the LANA, the bypassing method (also known as an envelope termination technique) can improve Ulna’s lip performance without increasing current consumption. 5. LANA components and the effect on PIP ; Any mismatch due to noise matching CIA/IL improves Input-PIP. Increasing LA reduces gain and improves Input-PIP, but watch for microwave oscillation with excessive inductance. ; CO can use to improve PIP- provides gain roll-off at 2*IF or 2*IF. ; Printed circuit board losses RE provide IQ stability while reducing PIP. RE less than 27 Q for about a db reduction in PIP. ; CO and CO provide a HOFF termination for IQ . Depending on spacing of signals seed to test PIP, values may not be large enough – may necessitate additional low frequency bypassing in the form of CO and CO.

Typical values are 0. 01 to 0. 1 if. ; The combination of CO/CO, CO/CO and CO/CO must provide low impedance at IF – Fl . May have to add resistance

between caps to decrease Q. ; CO and CO also used to minimize power supply noise from modulating the DC. ; Capacitor CO, CO and CO performs the low-frequency bypass function and an improvement in PIP of approximately 5 to 10 db can be expected by using this method. Using extra charge storage on the drain may see the same effect, but the exults are not nearly as dramatic. The closer together the two input test tones Fl and IF are in frequency, the lower frequency the product or beat tone (F 2 – F 1) is. Therefore, as input test tones Fl and IF come closer together, more capacitance is needed to achieve best possible bypassing of the low frequency product (IF – Fl). For a test tone separation of 1 Mash, 0. 1 if was found to be more adequate for this application. For best results, the transistor should see a low impedance path at low frequencies between this additional bypass caps and its terminals. For this reason, a the RFC from the DC bias network.

For example a value of NH for L 1, has negligible impedance up to tens of Mash, but provides enough impedance at 2 GHz to nearly isolate the gate of the transistor from the bias network within Ulna’s normal operating frequency range. It is important to note that bypassing the IF – Fl product as described here does not affect the compression point of the amplifier, but only the PIP (3rd-order intercept point). As a results, if this bypassing used, the general rule of thumb stating that are approximately a 10 db difference between PIP and 1 db gain compression point (Pled) is no longer valid. . Real issues in LANA design ; An LANA is a design that minimizes the Noise Figure of the system by matching the device to its noise matching impedance, or Gamma optimum (rope). ; Gamma optimum (rope) occurs at impedance

where the noise of the device is terminated. ; All devices exhibit noise energy. To minimize this noise as seen from the output port, one must match the input load to the conjugate noise impedance of the device. Otherwise the noise will be reflected back from the load to the device and amplified.

While this gives a minimum noise figure, it often results in slightly reduced gain as ell as possibility increasing the potential instabilities. Noise match often comes close to SSL 1 conjugate (SSL 1*) under non-feedback conditions. As a result, the input impedance to the amplifier will not be matched to 50 ohms. rope, as presented in data sheets, is the actual measured load at which the minimum noise figure is found. ; Noise Figure for BSTJ LANA increases more rapidly than FEET LANA, as Collector/Drain current is increased. Feet allows for better trade-off between high-linearity and low Noise Figure than BITS. A further complication on LANA design is that the input load of the amplifier is usually less than ideal. It is either connected to an antenna, which can change its impedance with changing the environment, or to a filter, which by very physics of a reflective network will have very bad match out of band. These mismatches could cause the device to become unstable out of band and some cases in band. As the gain of the device increases, the difficulties in yielding a stable design become increasingly more challenging.

To avoid overloading the LANA, an input filter is commonly used. Since the device is not matched to SSL 1*, the input of the LANA will not be 50 ohms. This can cause distortions in the pass band of the filter when connected to the input of the LANA, as filter are intended to operated in their characteristic impedance, typically 50 ohms. Printed inductors or

transmission lines are free as compared to SMS inductors, which typically cost 10 to 25 times as much as resistors or capacitors in volume. Printing an inductor is easy and results in highly repeatable results.

Printed inductors usually exhibit poor Q due to the loss dielectric, and, if a ground plane exists, they are no more than a high impedance transmission line. As shown a transmission line can replace an inductor to some degree, but inductors and high impedance transmission lines have a different trajectory on the Smith Chart. High impedance transmission line can be made to look more like printed grounded chassis. This is accomplished by removing the backside ground plane of the PC directly under the printed inductor.

In this case beware of digital noise coupling into the input of the LANA from circuitry on the opposite side. ; The next concern is what load impedance to match. Remember matching to the conjugate of SIS* is only valid if the input is conjugate matched. Since SIS is non- zero, whatever load is present to the input will cause the output load change. ; Another issue is stability, especially if a filter is going to be used at the input. The output port can potentially give difficulties since the input is very restricted by its match.

The designer must replace the ideal sources in the bias circuit and ideal values in the matching circuit with equivalent real components. This often presents the designer with a new set of problems. First, the bias network must be robust enough to function properly over a range of power-supply voltages and temperatures. This introduces additional complexity into the bias network. The real components in the bias network the resistors and

large capacitors operate at DC voltages, so frequency effects are not a problem.

The matching network, however, contains real capacitors and inductors that operate at RFC frequencies. Real components differ from ideal ones in several respects. First, real components have a price associated with them. There is a trade- off between price and performance of these parts. The competitiveness of today’s markets often forces designers to use inexpensive components in their designs. Real discrete components have a finite resistance called Equivalent Series Resistance (USER). The USER introduces losses that result in lower gain and noise figure.

Although typically only a few tenths of an ohm in value, USER will affect the matching networks. ; Discrete components also have a Q value, measured at a particular frequency that can contribute to unwanted resonance. ; High-Q networks are sensitive to variations in process, voltage, temperature, and component value. ; A component’s Series Resonant Frequency (SERF) is the frequency where it will behave erratically. For example, if an inductor is operated at or above its SERF, it might behave as a capacitor. To avoid this, select components where the SERF is much higher than the operating frequency. Also, leaded through -hole parts have leads that add series inductance to a design, and surface-mount parts have pads that add shunt capacitance to a circuit. ; Another issue is that of packaging a completed design. If the circuit is to be integrated and sold as an Integrated Circuit (C), it must be packaged. The package introduces several negative effects. In an ‘ C, the bond wires add unwanted inductance (L) and the bond pads add

unwanted capacitance (C). ; Isolation between pins in the package is also important.

Lack of pin -to-pin isolation in a feedback circuit can lead to major reliability problems and stability concerns. The additional inductance in the emitter of the collector-emitter section can severely degrade the noise figure of the circuit. ; Additionally, several grounds are usually needed to improve the performance of RFC circuits, but the package has a limited number of pins. After using the input, output, adequate design. All of these factors can degrade the circuit’s performance from the ideal, and the designer must carefully take them into account. . COSMOS LANA Design ; A few comparison characteristics between COSMOS and BSTJ Lana: o The DC currents of COSMOS and BSTJ Ulna’s are close; therefore the transcendence (GM) of COSMOS transistor is lower than the BSTJ one’s. O The GM/l ratio of COSMOS is lower than that of BSTJ. O In COSMOS technologies, a high Ft is achieved through a smaller CSS, while in BSTJ technologies the same Ft is obtained through a higher GM. O Smaller CSS means COSMOS tuned circuits tend to have higher Q, a disadvantage in outstanding component or process variation.

The COSMOS LANA input quality factor (independent of L’s) is defined as follows: There are two types of methods commonly used to design an LANA in COSMOS circuits: ; Common-Gate ; Cascade amplifier While the Common-Gate stage provides a wide-band input matching and is less sensitive to parasitic, it has an inherently high noise figure. Common-Gate COSMOS LANA ; With the increasing of the operating frequency, the parasitic transistor

capacitance CSS starts playing roles, which degrades the amplifier performance in the high frequency.