The butterworth low pass filter design marketing essay

Filters are widely used in electronic systems to emphasize signals in selected frequencies and reject signals in other frequencies. An ideal filter can change the relative amplitudes of the various frequency components and their phase relationships, without adding new frequencies to the input signal and changing the component frequencies of that signal. It is to say a filter is an electrical network that alters the amplitude and phase characteristics of a signal with respect to frequency. [1] So the low pass filter to be presented here is a filter which passes low frequency signals, and rejects signals at frequencies above the filter’s cut-off frequency.

There are a great number of different types of filter responses, in which the Butterworth response is the flattest pass band response available and contain no ripple. The attenuation is -3 dB at the cut-off frequency, and above the cut-off frequency the attenuation is -20 dB per decade per order. Butterworth filters are used to maintain gain flatness, which is very important, especially at low frequencies. [2]

As for the filter topologies, the Sallen & Key topology is used here to implement the second-order active filters due to its simplicity of the designs.

In this report, after introducing the relevant theory, the design process of a Butterworth low pass filter with 483 KHz cut-off frequency and 40 dB pass band gain is presented. From schematic to layout, the circuits are designed and simulated by using Cadence.

II THEORY

Op-amp design

Op-amps are fundamental building blocks used in many analogue circuits and systems. Fig. 1 shows the op-amp used in this filter, which consists of three stages:

opamp. jpgopamp-c. jpg

Fig. 1 Simply Op-amp with 3 Stages Fig. 2 The Schematic of Op-amp

A differential pair is used for the input stage. Second stage is a simple common source gain stage, which uses same Vbias as the differential pair. The third stage is a simple source follower and the output follows input with a level shift. [3] The schematic is shown in Fig. 2

Filter design

Higher-order filters can be constructed by cascading lower-order filters. To implement an even- order filter, n/2 second-order filter stages are required (n is the order of the filter). And for the odd-order filter, a first-order filter stage is added with (n-1)/2 number of second-order filters. The stages are normally arranged with the lowest Q near the input and the highest Q near the output to help avoid saturation, in which Q is the quality factor. [4] (Shown in Fig. 3)

even. jpg

Fig. 3(a) Even-Order Filters Consist of n/2 Second-Order Stages

odd. jpg

Fig. 3(b) Odd-Order Filters Consist of Second-Order Stages and Adding a First-order Stage

First-order low pass filter [5]

1. jpgFig. 4 First-Order Low Pass Filter

The transfer function of the first-order filter shown in Fig. 4 is

(1)

where K is the DC gain, fc is the cut-off frequency, and

(2) (3) (4)

It is clearly, R1 and C1 define the cut-off frequency while R11 and R12 define the gain.

Second-order low pass filter with Sallen & Key topology[6]

2. jpgFig. 5 Second-Order Low Pass Filter

The transfer function of the second-order filter shown in Fig. 5 is

(5)

There are four different simplification methods available in Sallen & Key topology. In this design, the filter components are set equal to simplify the circuit, which means both resistors and capacitors are assumed to be equal. Letting, , then the transfer function would be

(6)

Where (7), (8), (9),

(10), (11)

Similarly to the first-order filter, R and C define the cut-off frequency while R3 and R4 define the gain. However, in this design, the gain of the circuit now determines Q.

III DESIGN PROCESS

Butterworth Low Pass Filter Specifications [7]

The specifications of this Butterworth low pass filter are listed in Table 1.

Table 1 Butterworth Low Pass Filter Specifications.

Pass Band Edge Frequency

Stop Band Edge Frequency

Maximum Pass Band Ripple

Minimum Stop Band Attenuation

Pass Band Gain

483. 35 KHz

966. 70 KHz

3 dB

40 dB

40 dB

The design goal is to meet specification, minimize power consumption and minimize the area.

During the design, the primitive elements being used must select from the PRIMILB Cadence library. Specifically, nmos4 for N type Mosfets, pmos4 for P type Mosfets, cpoly for capacitors and rpolyh for resistors. What’s more, the dual supplies with a ground connection is recommended as power supply with VDD= 1. 67V, VSS=-1. 67V, GND= 0.

The Overall Design Flow

Fig. 6 shows the overall design flow in designing this Butterworth low pass filter. The detailed design process is presented below.

process. jpg

Fig. 6 Butterworth Low Pass Filter Design Flow

Op-amp Design, Simulation and Layout

The op-amp is designed based on the circuit shown in Fig. 2. Fig. 7 is the schematic view of the op-amp designed in Cadence using the specified components.

Fig. 7 Op-amp Schematic in Cadence

For the sizing of transistors in this op-amp, all lengths are set the same to 0. 6um, the widths are set as Table 2. [3]

Table 2 The Widths of Transistors in Op-amp (Units: um)

MP0

MP1

MP2

MP3

MP4

MP5

MN0

MN1

8. 75

8. 75

105

105

105

105

8. 75

8. 75

MN2

MN3

MN4

MN5

MN6

MN7

MN8

MN9

35

8. 75

52. 5

52. 5

50

175

98

175

After create the symbol view of the op-amp from the schematic, the schematic shown in Fig. 8 is used to do the simulation. A large feedback resistor R= 100M is added to establish DC bias point and the large capacitor C= 10uF help to removes AC signals fed back. Fig. 9 is the schematic view of the dual power supplies used in this design.

Fig. 8 Simulation Schematic of Op-amp Fig. 9 Dual Supplies

An AC sweep has been done and Fig. 10 shows the AC response from the output. The gain of the op-amp is over 70dB. At unity gain the phase margin is 180-101. 4 = 78. 6 degrees. The response is good so there is no need to further optimize the op-amp. The following step is to do the layout.

Fig. 10 AC response of Schematic simulation Fig. 11 Op-amp Layout

LayoutXL is selected to create the layout from the schematic view of op-amp. It can automatically place the transistors in the layout. Fig. 11 shows the completed layout with proper components place and wire routing. Following many attempts, the distances between the devices have been shorten and the area of the whole layout has been reduced, but not too small to cause DRC error and generate too many parasitic capacitances. The overall area of the op-amp layout is approximately 70*70 um2.

This layout passed DRC, and the default extracted model electrically matches the schematic. Then an extracted model with parasitic has been generate to do the post-layout simulation using the Hierarchy Editor. The result of the post-layout simulation will be far more realistic than the schematic simulation. Fig. 12 shows the post-layout simulation result, with

the same gain as the schematic simulation and a slight difference in phase margin at unity gain. It also confirmed the correctness of the layout. Fig. 13 is the extracted view of op-amp.

Fig. 12 AC Response of Post-simulation of Op-amp Fig. 13 Extracted Model of Op-amp

The power consumption of the op-amp is calculated by measuring the currents flowing through the dual power supplies (shown in Eq (12)). A transient simulation has been done to measure the currents.

(12)

From the schematic simulation, rms(Ivdda) = 0. 34970 mA, rms(Ivssa) = 0. 34970 mA. As for the post-simulation, the rms(Ivdda) and rms(Ivssa) are also both equal to 0. 34970 mA, that makes the power consumption of the op-amp P= 1. 16800mW.

Butterworth Low Pass Filter Design

For convenient, the order of the filter can be computed by using Matlab.

Function [N, Wn] = BUTTORD(Wp, Ws, Rp, Rs, ‘ s’) returns the order N of the lowest order analog Butterworth filter that loses no more than Rp dB in the pass band and has at least Rs dB of attenuation in the stop band. Wp and Ws are the pass band and stop band edge frequencies in radians/second.

Letting Wp= 2*pi*483350, Ws= 2*2*pi*483350, Rp= 3, Rs= 40, the function returns N= 7. This means the filter designed here should be a 7-order Butterworth low pass filter.

According to the theory introduced at the beginning of the report, 7-order Butterworth low pass filter can be realized by 1 first-order low pass filter and 3 second-order low pass filter. Using Sallen & Key architecture for the second-order filter stages, the filter circuit is shown in Fig. 14.

F. jpg

Fig. 14 7-order Butterworth Low Pass Filter

What to do now is to calculate the values of the passive components in the circuit. The normalized 7-order Butterworth polynomial is

(13)

So the transfer function of 7-order Butterworth low pass filter is

(14)

Where K is the pass band gain that makes 40dB= 20logK so K= 100.

Start from the first second-order filter stage. Using Eq (6), the transfer function of this stage is

(15)

where. From Eq (15), it is clearly that,. So,,.

Similarly, the parameters in the second and third second-order filters can be calculated using the same method. The results are listed below.

”

”

The calculation of the first-order filter stage is a litter different. Using Eq (1) and (14), the transfer function of this stage is

(16)

So .

However, the gains of the second-order filters were determined by the architecture and the only way to achieve the expected total gain is to adjust the gain in the first-order filter stage.

For , so that, .

Set the value for C and solve for R. Taking values of all the capacitances as 10pF would be a suitable starting point. The values of all the passive components in the circuit are shown in Table 3.

Table 3 Ideal values of all the Passive Components in the Filiter

C1

10pf

C2

10pf

C3

10pf

C4

10pf

R1

32. 9 kÎ©

R2

32. 9 kÎ©

R3

32. 9 kÎ©

R4

32. 9 kÎ©

R11

1 kÎ©

R21

1kÎ©

R31

1kÎ©

R41

1kÎ©

R12

17. 635kÎ©

R22

0. 198 kÎ©

R32

0. 753 kÎ©

R42

1. 555 kÎ©

A verilog-A model of the level one op-amp is created, the code is included in the appendix in the end of the report. A cascaded filter circuit using this model and all the ideal passive components listed above is shown in Fig. 15. An AC analysis has been carried out to test the frequency response of this circuit. The simulation result shown in Fig. 16 tells that there is no big mistake in the realization of the passive and active components in this circuit. However, further optimization should be done to make the response closer to the specification.

Fig. 15 Schematic of 7-order Butterworth Low Pass Filter using Verilog-A model Op-amp

Fig. 16 AC Response of the Filter Shown in Fig. 15

Fig. 17 shows the schematic view of the filter circuit using the op-amp designed before and the passive components from PRIMILB Cadence library. It would be a little different from using the verilog-A model op-amp and ideal passive components. The rpolyh and cpoly from PRIMILB library have their own predetermined values, so the component with proximate value would be selected when an ideal value is needed. In this case, 10. 0015pf cpoly is used instead of the calculated capacitance with exactly 10pf.

Fig. 17 Schematic of 7-order Butterworth Low Pass Filter

Fig. 18 is the schematic of filter simulation circuit. In order to get a more accurate cut-off frequency and pass band gain, some values of the passive components have been slightly changed after repeated experiments of adjustment and testing. Fig. 19 shows the AC response of the circuit with parameters' values listed in Table 4.

Fig. 18 Schematic of Filter Simulation Circuit Fig. 19 AC Response of the Filter

Table 4

C1

10. 0015pf

C2

10. 0015pf

C3

10. 0015pf

C4

10. 0015pf

R1

31666. 7Î©

R2

31666. 7Î©

R3

31666. 7Î©

R4

31666. 7Î©

R11

1 kÎ©

R21

1kÎ©

R31

1kÎ©

R41

1kÎ©

R12

17. 635kÎ©

R22

0. 198 kÎ©

R32

0. 753 kÎ©

R42

1. 555 kÎ©

Floor-plan has been determined when doing the filter layout. Fig. shows the final layout of this filter and Fig. is its extracted model. The layout passed DRC, and the default extracted model electrically matches the schematic. The whole area of the filter is approximately 340*400um2.

Similarly, a post-simulation has been done to test the correctness of the layout. But this time, the ultimate goal of doing post-simulation is to confirm the AC response from post-simulation conforms to the specification.

Once again, the values of the passive components in the filter circuit have been varied in order to make sure the response of extracted model simulation meet the specification. After a number of experiments, the values have been determined and shown in Table 5.

Table 5

C1

10. 0015pf

C2

10. 0015pf

C3

10. 0015pf

C4

10. 0015pf

R1

31166. 7Î©

R2

31166. 7Î©

R3

31166. 7Î©

R4

31166. 7Î©

R11

1004. 08Î©

R21

2002. 04kÎ©

R31

1004. 08kÎ©

R41

1004. 08kÎ©

R12

17798Î©

R22

397. 959Î©

R32

753. 061Î©

R42

1567. 35Î©

The AC response of post-simulation is shown in Fig. It seems different frequency ranges of AC sweep may lead to different results because of different sweep accuracies. Fig (a) shows the frequency range from 10 Hz to 10 MHz while (b) has a frequency range from 10 KHz to 1. 5 MHz.

The curves show that the pass band gain of this filter is 40 dB with cut-off frequency 483. 4 kHz, the stop band edge frequency 966. 7 kHz corresponds to the gain around -1. 15 dB, which means the stop band attenuation is more than 40 dB. All the features in the AC response exactly conform to the specification.

Fig(a)(b)

Compared with the AC response of schematic simulation (using the parameters' value in Table 5) shown in Fig , the existence of parasitic capacitances result in a slight difference between the cut-off frequencies of post-simulation and schematic simulation.

Fig(a)(b)

The power consumption is calculated according to Eq (12).

From the schematic transient simulation of the filter, rms(Ivdda) = 1. 39332 mA, rms(Ivssa) = 1. 39939 mA. As for the post-simulation, rms(Ivdda) = 1. 39332 mA and rms(Ivssa) = 1. 39939 mA, so the power consumption of the filter P= 4. 6638mW.

IV PROBLEMS AND IMPROVEMENTS

The design process of this Butterworth low pass filter and the simulation results has been reported. Here are the problems met during the design and by analyzing the causes for these problems, solutions and measures for improvement are proposed.

The main problems came forth in this filter design is during the layout design. Lots of time and energy has been spent on doing a layout with better performance. At first, the DRC check and error correct cycle took plenty of time. DRC errors are well explained so it is not too hard to correct them. After dealing with DRC errors, great efforts have been made to minimize the area. However, the AC response of the former design with small layout area turned out not as good as expected. The AC response from post-simulation of the filter is far from that of schematic simulation (about a gap of more than 15 kHz between cut-off frequencies). Realized the main cause of this problem is the existence of too many parasitic capacitances, measures have been taken to reduce them. One way to decrease parasitic capacitances is to increase the distance between components and wires, however, the drawback is the increase of area. A new layout of filter has been created with longer distance between metal wires (shown in Fig.). This layout simulated

better with a gap of less than 9 kHz between cut-off frequencies of schematic model and extracted model (according to Fig. and Fig.).

V CONCLUSION

This report proposed a design of Butterworth low pass filter with 483 KHz cut-off frequency and 40 dB pass band gain. The design specification has been well achieved. By completing this study, it can be concluded that higher-order filters can be realized by cascading lower-order filters; and the second-order active filters with Sallen & Key architecture is a good choice in reducing the complexity of circuit; sizing for each component is very important while doing the schematic design for layout purposes; parasitic capacitances should be taken into consideration when doing floor-plan for layout.

Admittedly, the Butterworth low pass filter has been designed in this coursework is far from perfect and it requires further optimization. In future study, it is possible to figure out ways to reduce power consumption and layout area without increasing parasitic capacitances.