

Cot controlled buck converter essay sample



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The effect of equivalent series resistance (ESR) of an output capacitor on the performance of a constant-on-time (COT)-controlled buck converter is studied and a pulse bursting phenomenon is revealed. It indicates that the ESR of the output capacitor is one of the key factors causing pulse bursting phenomenon in COT-controlled buck converters, and the critical ESR is derived via. It is pointed out that, when the ESR of the output capacitor is smaller than the critical ESR, pulse bursting phenomenon occurs, otherwise it disappears. Simulation results are provided to verify the theoretical analysis results.

INTRODUCTION

The control techniques of switching dc-dc converters can be generally divided into the following three ways. 1) Constant-frequency control, such as pulsewidth-modulation-based voltage-mode control and current-mode control 2) Variable-frequency control, such as output-voltage-ripple-based control like constant-on-time (COT) control or constant-off-time control 3) Hybrid control

To improve the transient performance and to simplify the controller design of switching dc-dc converters, COT control has attracted much attention recently. COT control is simple to implement and easy to design, without an error amplifier and its corresponding compensation network.

In this paper, pulse bursting phenomenon of a COT-controlled buck converter is revealed via both time and s-domain analysis, the ESR of the output capacitor for the pulse bursting phenomenon is obtained. Simulation results are provided to verify the theoretical analysis.

PULSE BURSTING PHENOMENON

A) Review of COT Control

COT controller consisting of a comparator, an Reset-Set(RS) trigger, and an ON timer. From the wave forms, once the output voltage V_o decreases to the reference voltage V_{ref} , the RS trigger will be triggered to turn on the power switch S to increase V_o , after the preset COT interval T_{on} , the RS trigger will be reset to turn off S , and it will be turned on again when V_o decreases to V_{ref} to initiate the next switching period.

B) Pulse Bursting Phenomenon Analysis

At the end of the COT interval that is at the time instant when S is just turned off, V_o should be higher than V_{ref} to maintain normal operation. Otherwise, after a very short off time caused by the reset signal of RS trigger, will follow consecutively until V_o increases to higher than V_{ref} . In this case, pulse bursting phenomenon will occur, with large inductor current and output voltage ripples. The output voltage variation of a buck converter is composed of voltage variation across the output capacitor and its ESR resistor. The voltage variation across the ESR resistor is in proportion to the inductor current. That is the voltage across the ESR resistor will increase during the time interval when S is turned on, which helps to make the COT - controlled buck converter operate in normal operation. The voltage across the output capacitor may increase or decrease when S is turned on, depending on the relationship between the inductor current and load current. When the inductor current is lower than the load current, although S is on, the output capacitor will be discharged, which makes its voltage

decrease. Thus when the output voltage variation is dominated by the output capacitor voltage variation, V_o may be lower than V_{ref} during the time interval when S is turned on. In this case, normal operation cannot be ensured, and pulse bursting phenomenon will occur.

C) Critical ESR For Pulse Bursting Phenomenon

When the voltage V_{ESR} across the ESR resistor is large enough to dominate the output voltage variation, the COT-controlled buck converter operates normally without pulse bursting phenomenon. When V_{ESR} is not large enough to dominate the output voltage variation, the pulse bursting phenomenon occurs. After some COT intervals, S is turned off for a relatively long time, resulting in large inductor current and output voltage variation. Between the adjacent COT intervals there is a very short off time caused by the reset signals of the RS trigger. If the slope of $-V_{ESR}$ is less than or equal to that of V_c ripple at the time instant when S is just turned off, normal operation can be ensured, and no pulse bursting phenomenon occurs. Otherwise, the buck converter will operate abnormally and pulse bursting phenomenon will occur. The slopes of $-V_{ESR}$ and V_c ripple at the time instant when S is just turned on can be obtained as

$$d(-V_{ESR})/dt|_{t=nT_s} = -d(R_{ESR}i_L - I_o)/dt|_{t=nT_s}$$

$$= -R_{ESR}V_{in} - V_o/L$$

$$dV_c/rippledt|_{t=nT_s} = i_L - I_o/C|_{t=nT_s}$$

$$= -\Delta I_L/2C$$

$$= -V_{in} - V_o/T_{ON}2LC$$

respectively, where ΔI_L is the peak-to-peak value of the inductor current in steady state. Equating the above two equations, the critical ESR R_{ESRC} can

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be obtained as

$$RESRC = TON/2C$$

To ensure normal operation, RESR must be greater than RESRC. Otherwise, the COT-controlled buck converter will work abnormally, and pulse bursting will occur. From the above equation, we can further have

$$\tau = RESR \geq TON/2$$

That is once TON is designed, the time constant τ of the output capacitor must be designed to be greater than TON/2

COT controlled buck converter a) Circuit block diagram b) main operation wave forms

Waveforms under two cases a) with large RESR and b) with small RESR

SIMULATION AND EXPERIMENTAL RESULTS

MATLAB/ SIMULINK MODEL for COT -Controlled Buck converter

Time-domain simulation results of the COT-controlled buck converter with RESR = 5m Ω

Time-domain simulation results of the COT-controlled buck converter with RESR = 2 Ω

Variable	Signification	Value
Vin	Input voltage	15V
VO	Output voltage	5V
L	Inductance	66.7mH
C	Capacitance	2.498mF

$R|$ Load resistance| 5Ω |

$T_{on}|$ Constant on-time| $6.67ms$ |

PARAMETERS OF THE COT- CONTROLLED BUCK CONVERTER

ANALYSIS AND DESIGN

Using $V_{in} = 15V$ and $V_O = 5V$

$V_o = kVS$, From this equation $k = 1/3$, ie $T_{ONT} = 1/3$

Here T is taken as $20ms$, then $T_{ON} = 6.67ms$

Using the formula, $C = \frac{Vsk(1-k)\Delta V_c}{L f^2}$ $C = 2.498Mf$

$L = \frac{Vsk(1-k)\Delta I_f}{L} = 66.7mH$

$R_{ESRC} = T_{ON}/2C$ $R_{ESRC} = 1.33\Omega$

Here the simulation results are shown with $R_{ESR} = 5m\Omega$ and 2Ω One of the equivalent resistance greater than critical value and the other is less than R_{ESRC} Limitation: Here the MATLAB/SIMULINK Model does not contain flip flop , comparator, reference voltage as shown in the circuit block diagram, because of the connection difficulties in MATLAB. So the pulse bursting is not completely visible in the simulated wave forms. Based on the reference paper the simulated waveform is

a) With $5m\Omega$ b) With $20m\Omega$

CONCLUSION

In this paper, a pulse bursting phenomenon , which is a complex nonlinear phenomenon , in a COT -controlled buck converter has been revealed . It is indicated that the ESR of the output capacitor has great effect on the control performance of the COT-controlled buck converter . The investigation results presented in this paper provide a useful guideline for the design of COT-

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controlled buck converters, eg: ceramic capacitors are usually not appropriate as output filter capacitor they have very small ESR.

REFERENCES

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