Thyristor ram essay

THYRISTOR RAM Muktesh Waghmare, Raman Gaikwad 1: Principle: Thyristor is well-known for its high-current drive capability and its bi-stable characteristics. It has been widely used in power electronics applications. With the exponential advances in CMOS technology tiny thyristor devices can now be easily embedded into conventional nano-scale CMOS. This enables the creation of a memory cell technology with features that include small cell size, high performance, reliable device operation, and good scalability. Use of thyristor provides a positive regenerative feedback that results in very large bit cell operation margins.

The difference is that the four-transistor CMOS latch of a 6T-SRAM is replaced by the PNP-NPN bipolar latch of a single thyristor device, which reduces cell area dramatically and enables high-density macros. 2: Need of the technology: There has always existed a fundamental performance-density trade-off between SRAM and DRAM, the only two commercially viable volatile memory technologies. SRAM provides high performance at the expense of a large cell area, while DRAM provides high density but with low performance. The internal latch of a SRAM cell comprises of four-six transistors.

This degrades the packaging density of a SRAM based memory. The performance limitation of DRAM is primarily a result of using a passive capacitor as the storage device without an internal gain. DRAM read operation is therefore destructive and the data retention is highly leakage sensitive. Destructive read requires the use of a read and write-back operation for every memory access or refresh operation, slowing down the random cycle time. Since a T-RAM cell consists of only two elements (a

thyristor device and an access FET), its cell area is significantly smaller than 6T SRAM.

The slow turn-off speed of a conventional thyristor is addressed in a T-RAM cell through the use of a thyristor structure, called thin capacitively coupled thyristor TCCT). 3: Working: The fundamental component of a thyristor based cell structure is the internal thyristor latch. A CMOS-based thyristor device known as a Thin Capacitively Coupled Thyristor (TCCT) (Fig. 1) has been introduced as a novel switching device for high-density high-performance memory applications in thyristor based memory cells.

The switching speed of the TCCT device is determined by various device parameters such as npn and pnp bipolar gains, gate to-p base capacitive coupling ratio, and carrier lifetime ? in J1. Due to the unique gate coupling mechanism, the excess carriers in the p-base are removed at the falling edge of the gate pulse without carrier recombination; however, carriers in the n-base need to be removed by recombination. Therefore, the carrier lifetime in the J1 junction becomes a limiting factor for the turn-off switching speed. When ? is reduced, carriers in the n-base are more quickly recombined, resulting in improved turn-off speed. [3]

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The gain of bipolar transistors increases with temperature. Indium is employed as the p-base dopant species in order to modulate the temperature coefficient of NPN gain and stabilize thyristor characteristics over a wide operating temperature range. The base of an NPN bipolar transistor is typically doped with boron, which is nearly fully ionized over the operating temperature range of most semiconductor devices. Indium is known to have an acceptor level which is 156 meV above the top of the valence band of silicon. As a result, the fraction of ionized indium atoms increases with temperature, esulting in reduced gain. Such a thyristor (TCCT) that has good thermal stability, large switching speed and a small fabrication size is used to create memory cells. Two possible thyristor cell structures for memory devices are as follows: 3. 1: Thyristor based S-RAM: T-RAM consists of a thin vertical thyristor with a surrounding MOS gate as the bi stable element and a planar NMOSFET as the access transistor. A novel gate-assisted switching mechanism is used in T-RAM which enables the thyristor to switch at a high speed and a low voltage level. 5] : Write operation: Both WL1 and WL2 are high. The first word-line will control the access gate while the second word-line will control the thyristor gate. When writing a “ high”, the bit-line BL is set at low, and both word-lines WL1, WL2 are switched on. At this moment, the thyristor behaves like a forward biased PN diode. After a write operation, both gates are shut off, and a “ high” state is stored in the

thyristor. When writing a “ low”, the bit-line BL is set at “ high” state, and both word-lines WL1, WL2 are switched on.

At this moment, the thyristor behaves like a reverse biased diode. After the write operation, both gates are shut off, and a “ low” state is stored in the thyristor Read operation: In a read operation, only the first word-line WL1 is activated. The bit-line current is sensed by a sense amplifier. A large current will indicate logic ‘ 1’ and vice versa. During the stand-by ‘ ON’ state the holding current to the thyristor is provided by the sub-threshold current of the access transistor Simplified diagram and waveforms: 3. 2: Thyristor based D-RAM:

CONCEPT: The new TCCT DRAM memory cell is constructed using three control lines; bit line, word line, and write enable line. The anode node is connected to a bit line (anode line) and the cathode node is connected to a word line (cathode line). The gate poly line itself functions as a write enable line. [4] For write 1, gate line is pulsed while cathode line is held at ground level, triggering the TCCT device to latch. The bias scheme for write zero operation is the same as write one except that bit line voltage is kept low (Vwrite0) so that the pulsing of the gate line switches the TCCT into its blocking state.

For Read operation, the cathode line is held low and the change in the voltage or the current of the bit-line is read into a sense amplifier. The write enable line at the gate is not active in read operation. In standby mode, both anode and cathode lines are at Vdd and the stored cell data is maintained by the charge state of the P-base of TCCT. Waveforms: 4: Typical cell

characteristics: 4. 1: Thyristor S-RAM: Cell area: 0. 56µm2 (130 nm SOI technology) Read operation: <1. 7 ns Write operation: <2 ns

Read current distribution: 40µA/cell (logic ‘ 1’), < 10pA/cell(logic ‘ 0’) [2] 4. 2: Thyristor D-RAM: Cell area: 0. 44µm2 (130 nm SOI technology) Write_zero time: 2ns Write_one time: < 0. 5 ns Read current distribution: 120µA/cell (logic ‘ 1’), < 10pA/cell(logic ‘ 0’) Data zero refresh time: 266 85C Data one refresh time: not required [2] 5: Future prospects:

The Thyristor-RAM macro provides the highest combination of performance and density among all embedded memories solutions. A Thyristor-RAM macro matches 6T-SRAM in performance while providing 2-3x higher macro density, and lower power consumption. The Thyristor-RAM is fully CMOS compatible and can be readily integrated with a baseline CMOS technology on either Bulk or SOI substrates without any impact on the baseline technology/transistors. Thyristor –RAMs have been fabricated and have proven their efficiency in 130 nm (die size) SOI mode. Thyristor DRAMS are now targeting 45 nm, 32 nm and 22 nm mode.

In future, Thyristor-rams can be used to reduce the chip size or to increase the capacity of cache memory in processors. Cell size comparison of t&s-ram There are some drawbacks that may limit the adoption of thyristor based memory storage cells as SRAM replacement in high speed memory applications. T-RAM states that the TCCT test chip was fabricated on the standard 130 nm high performance SOI process with 16 additional process

steps added. However, most of the steps are simple implant-only steps, and the same mask set is used for several of the additional processing steps.

Moreover, the additional processing steps are all relatively simple, low-temperature steps in the backend, and do not impact the (MOS) transistor stack formation. A second drawback that could potentially limit the adoption of the thyristor cell is that thyristor memory are rather susceptible to soft errors caused by single event upsets (SEU), just like SRAM cells. The SEU can inject a current pulse into the P-base and mimic the write pulse of the write cycle in the Thyristor. References: [1] http://www. t-ram. om/technology/Publications. html [2] http://www. t-ram. com/technology/documents/HotChips2007_TRAM. pdf [3] IEEE International conference “ Optimization of Substrate Doping for Back-Gate Control in SOI T-RAM Memory Technology” [4]IEEE International Electron Device Conference (IEDM)” A novel capacitor-less DRAM Cell using Thin Capacitively-Coupled Thyristor (TCCT)” [5]IEEE International Electron Device Conference (IEDM) “ Fully Planar 0. 562? m2 T-RAM Cell in a 130nm SOI CMOS Logic Technology for High-Density High-Performance SRAMs”