Silicon field effect transistor (ncsifet) in beol

Tremendous research efforts are ongoing in order to implement and add further functionalities to computing compounds in CMOS chips. Thus, a challenge is imposed to compete the existing devices in terms of cost and performance. In this project, I propose a novel and low cost approach for nanocrystalline Silicon Field Effect Transistor (ncSiFET) based memory selector implemented in BEOL. During this thesis, the potentiality of this technology in terms of performance and production cost will be established.

Targeted technological applications : Memory selector transistor

One of our research group activities in 3IT consists on the development and integration of RRAM with a Complementary Resistive Switch (CRS) planar configuration in the BEOL of CMOS circuit. My research activity will focuses on memory selector fabrication needed to carry out the read operation as subsequent and complementary function. Several technological approaches have been proposed to fulfill this function with different physical concepts, such as diodes, volatile switches, nonlinear devices and transistors. (cf. figure I. 1). Owing to the planar configurtion and the nanodamascence fabrication approach of RRAM, our transistor device (ncSiFET) will benefit from the process compatibility, so that it can be implemented in 3D BEOL integration and connected in serial to minimize parasitic leakage current from unselected cells during a read operation, to provide sufficient on-current for the switching of the selected cell and to prevent frequent interference operation and readout errors. The selector and the memory element should be compatible in term of scalability to enable limited leakage current from the unselected memory elements along read and write operations.

The requirements for a RRAM selector present several challenges for appropriate integration in a low-cost CMOS-compatible stackable process. A low processing temperature under 400 °C must be respected to enable the compatibility with 3-D integration in BEOL. The implementation of selector devices requiring additional process steps is accompanied with large device area and power dissipation. Moreover, the selector devices can cause a decrease in the current and a slower read operation. A compatibility in terms of in terms of operation polarity (unipolar/bipolar) and switching speed between memory elements and selector devices must be established [2]. Others aspects concerning the reliability such as cycling endurance and variability should be taken in consideration.

Required electrical performances

A good selector needs to satisfy multiple requirements which are essentially derived from circuit performance aspect. The previously achieved on/off ratio = 10^{4} with our (ncSiFET) [3] can be an asset for memory selector applications since it is on a par with many silicon transistor based selectors [4]. This ratio should be improved up to 10^{6}, to further enable the operation of large arrays in the architecture. Moreover, a 2. 5 Î¼A/Î¼m value as on-current in our device [3], which can be further enhanced, fits well with the range of requirement to sufficiently control the memory operation without speed restriction [5]. While threshold voltage needs to be minimized to enable the reduction of the operation leakage. These properties makes the transistor an effective selector as isolation switch and current limiter. A selector should be able to provide enough drive current as needed for SET

and RESET operations of the resistive memory cell. Interestingly, a threshold switching selector device has proved to be efficient for solving the leakage current problem with a low off current <100 pA/Î¼m [6]. This characteristic makes the (ncSiFET) very suitable candidate as low leakage memory selector with a demonstrated I off of about 30-120 pA/Î¼m [3]. In contrast, our (ncSiFET) suffers from a relatively high S. S value which should be improved to better ensure the selection function execution. The selector device should present a comparable operation polarity with the memory structures. The linearity and symmetry in the selector device characteristics are important parameter for the selection functions. Selectors with stronger exponential dependence have proven to be more suitable. It is worthy to note that I-V characteristics of (ncSiFET) has proved a bipolar operation with high symmetry behavior and a current rising exponentially with the voltage [3].

Taking all these considerations in account, one can say that (ncSiFET) device owns promising characteristics and relevant potential to be integrated in BEOL for RRAM memory selection applications. In table I. 1, we present further characteristics in as speed, temperature and electrical performances that should be also taken in account during the development of our device. Comparison with technological competitor

Silicon transistor based selector : The main advantages for this kind of transistors that enable self-compliance are their high ON/OFF ratio with large drive current, appropriate threshold voltage and low power consumption. However, transistor-based selectors present drawbacks in terms of large dimensions and complicated process fabrication [4]. Poly-Si material has been replaced by high quality epitaxial PN regions on crystalline Si, in order

to achieve high Ion/Ioff ratio up to 10^8 and large on current over $10MA/cm^2$ beneficial for SET/ RESET operation and rectifiying ability [7], but, these unipolar configurations are not compatible with bipolar switching mode resistive memories. The NPN structure has been proposed to overcome the polarity issue with I on /I off ratio of about 4700 [8]. However, the main limit for these technologies is their high process temperature, thus, unsuitable for sub-400 â-¦C BEOL integration. Metal-oxide schottky diodes: Different compositions of metal and oxides, such as Pt/HfO 2 /ZrO 2 /TiN or Ni/TiO 2 /Ni have been proposed [6]. The conduction mechanism assumed to be based on Schottky emission at the mateal/oxide interfaces [8]. It was demonstrated that (MIM) incorporating thin oxide film can provide non-linear I-V curve. These configurations are compatible with bipolar switching and suitable with 3D-stackable BEOL integration. However, only low drive current density of about $1MA/cm^2$ is reached. Nonlinear devices: Considering the requirement to achieve both high current at high voltage as well as very small current corresponding to low voltages, nonlinear devices have been proposed.

For all the varieties of this category presented in fig. 1, the complexity of fabrication process and the material selection remain difficult challenges for large area production and integration [4]. Thin film transistor (TFT): As an example, RRAM (Ti/Oxide stack/Pt) connected with thin film transistor (transparent amorphous oxide semiconductor (TAOS)) architecture demonstrated good results as current limiter with a storage capability controlled by the amplitude of the TFT gate voltage [2]. The TFT as a technology benefit from the reduced temperature, relatively simple and low cost fabrication process. However, carriers mobility in the channel is the

main issue that cause significant impact on the electrical properties of the resulting device. The transistor performances are severely affected by high defects density and carrier trap sites which strongly depend on the crystallinity, the quality of silicon thin film (a-Si, Poly-S or nc-Si). This is a common problematic to our ncSi channel. (ncSiFET): Our proposed transistor technology is based on nanodamascene approach, with a nanocrystalline silicon island as a channel separated from metal S/D by a thin tunnel oxide. A proof of feasibility with promising electrical performance is already demonstrated [3]. The overall process will be performed at low temperature (<400°C) to be compatible with BEOL monolithic integration. The existing platform in 3IT in terms of tools and materials will be an essential asset for the fabrication and the development of our proposed technology. The potential application of (nc-SiFET) as a transistor based memory selector will be demonstrated.

The aim of this project is to perform a cost-effective selector device compatible with our resources at 3IT. In this framework, strain effects are quite important for electronic transport in the channel, in other word, switch frequency and the reliability over time. Thus, this important aspect should be taken in account in order to establish the transistor characteristics and to fulfill the requirement for the realization and the application as a memory selector device. One of our project targets is to establish a strain method compatible with high-k/metal top gate configuration. Strained channel should be carefully designed through process conditions and device geometry.

Channel residual strain effects Residual strain could be either mechanical/intrinsic during the film growth and upon technological process

or thermal due the differences in expansion coefficient between materials or the auto-heating during the device operation. a) On transport properties in conductor channel For crystalline silicon channel, the strain in the channel of nanotransistor leads to the stretching of atoms bonding in silicon layer. The displacement of silicon atoms can reduces the impact of atomic forces that interfere with the electrons movement and weaken scattering phenomena allowing lower resistance and better mobility (cf. fig II. 1). Charge carriers can move faster in the strained channel resulting in better conductivity and low power consumption. In fact, stress induces a change and degeneracy in the energy bands level of the silicon atoms, causing an anisotropy in effective mass of electrons. Then, light mass and minimal scattering are the main factors for better mobility (Î¼= eÏ„/m*) [1]. Due to this anisotropy, the effect of strain depends on its direction with respect to the source-drain current path [2]. On the other hand, the deposition process of nSi-thin film leads to residual strain in the layer (tensile or compressive). For example, it was reported that the conductance of the amorphous material a-Si: H channel in TFT transistor increases with tensile stress while it decrease with compressive one [3]. In our nc-SiFET device, channel consists on isolated nc-Si 50nm-length and less than 20nm-thick island deposited and patterned using a combination of e-beam lithography and ICP-etching process. This channel embedded in nanopattern undergo a thermal annealing and Ti metal deposition before (CMP) polishing process leading to confined island from both side of the metal nanowires. Dielectric gate layers (Si 3 N 4) or high-k insulator (HfO 2 , Al 2 O 3 …) can be incorporated on the top of the structure in our process followed by gate deposition. In our project, metals materials can be deposited using evaporation or sputtering techniques, whereas,

dielectric layers can be fabricated by PECVD, LPCVD, sputtering or ALD. It is worthy to note that the induced residual strain of each region strongly depend on the choice of the deposition technique, process parameters, layer thickness as well as thermal post treatment. All these process specifications strongly affect the transport properties of the channel. Hence, a careful analysis of the channel mobility based on Hall effect measurements as a function of different process specification should be addressed (figure II. 2). A design of experiments would be performed jointly with the process fabrication. In this framework, several local strain techniques have been employed that can resemble our project. It was reported that shallow trench isolation technique -or box isolation technique- consisting on a sequence of trenches patterning to be filled by a deposited materials and removal of excess parts using CMP, creates isolation and can exert compressive stress on the channel [5]. Also, SiN capping layers on top of the gate with intrinsic stress can induce strain into MOS channels and enlarge the distance between atoms underneath the gate which enhance the electron mobility [6]. Based on these reported results, we can assume that our sequence of fabrication processes can induce further stress on the nanocrystallline silicon island channel. In order to precisely identify the effects of strain on our (ncSiFET) channel transport, we should take in account the contribution of all the steps that can take part of the channel residual strain in our process i. e nanoscale island embedded in the trench, thermal annealing, chemical mechanical polishing and the effect of capping layer stack.

On conduction mechanism between the electrical contacts and active region

The strain in the active layer of the channel can induce variations in terms of band gap, electrons effective mass, affinity and the density of states. It is proved that strain can cause a local band gap shrinking and a change in bands form along the channel [7]. Based on Kane model for band to band tunneling, the current is a function of band gap and effective mass change [8]. Hence, we can assume that the induced strain in our island channel can promote the conduction mechanism by direct tunneling through the potential barrier lowering. For our structure, inducing strain in (ncSi) channel can alter the potential barrier, state density and charge population between the thin tunnel oxide / ncSi interface as well as the gate dielectric/ncSi interface in our (ncSiFET) device. The reduction of a-Si island resistivity can enhance the contact resistance between the island and Ti source and drain terminals.

I. 2 Deposition methods : comparison In our case, the channel is a nanodimensional island deposited in a trench. For such nano-topography, uniform thickness on non-planar surfaces with step conformal coverage, space filling and damage-free process are required. In general, the evolution of stresses in thin films is a dynamic competition between tensile and compression effects during deposition. The strain in the film depends on different criteria such as grains size, micovoids, disorder. species mobility and deposition rate. Stress varies significantly with process conditions. At 3IT, several deposition techniques are available either chemical of physical based processes. We discuss the implications of each techniques on the nanodimensional (nc-Si) island strain as well as distribution and filling aspect.

LPCVD: based on heat activation at high temperature (> 500° C). Low gas pressure reduce gas-phase reaction which lead to low deposition rate and cause particle clusters. LPCVD Si thin film are isotropic and compact, but with poor step coverage [9]. Such high temperature and low deposition rate lead to the relaxation of the ordered film and thus, the annihilation of strain effect. Thermal or e-beam evaporation: requires heating or electron bombardement of source material to reach evaporation and transform into the gaseous phase (low energy atoms ~ 0. 1 eV) and then condensed and adsorbed on the substrate surface. The deposited film is characterised by poor uniformity and density with stoichiometrical problem due to the diffference in vapor pressure [9]. This process is better dedicated to thin film rather thick one, and chracterised by small strain effect at the initial stage of the growth [10].

Sputtering: employs the bombardment of a solid target by energetic particles gas ions (1 – 10 eV). Despite the good uniformity and stochiometry, this process gives rise to dense film with poor directionality [9]. In sputtered films, the ion bombardment of the surface at the initial stage of the film growth may lead to high strain aspect consisting on quite large compressive stresses where a tendency of film edges expansion is contracted back by the substrate [11].

PECVD: species decomposition can be carried out at lower temperatures (around 300 ° C) with high deposition rates and energetic species with high sticking coefficient. This process provides good film quality with conformal aspect and good step coverage [9]. The resulting film at such low temperature and high deposition rate is prevented from relaxation and

remains in strain, unlike high temperature process. Moreover, similar to sputtering technique ion bombardement may lead to further strain. The lack of surface diffusion may induce a high voids concentration which induce further strain in the film [10]. The interaction of atoms in the channel amorphous silicon film creates tensile strain, whereas the insertion of atoms causes compressive stresses [12]. Taking all the mentionned specifications, we may confirm the potential of PECVD technique to fabricate for nanodimensional ncSi channel island in nanotrench with interesting strain characteristics.

In order to fulfill the cost and performance requirements of (ncSiFET) transistor for memory selector application (vs state of the art), process development and device improvement are demanded. In this project, we pay special attention to physical dimensions and materials properties that determine the characteristics of our devices.

Improvements of (ncSiFET) transistor

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Before citing the general strategy for device improvements, we present in figure III. 1 the proposed structure accompagned with an overview about the electrical characteristics of (ncSiFET) transistor.

*Channel: – enlarge the grains size (> 80nm), minimize defects density inside the grain => optimization of a-Si deposition + RTA annealing + post-deposition H 2 plasma /Ge incorporation

-form narrow channel of about ~100 nm in the range grain size, making sure to avoid the effects of the short channels => EBL patterning of 100nm-box size

*Tunnel oxide: longer exposure duration up to 2 h to ambient air + annealing => more compact film with less defects and better stoichiometry

*Gate dielectric: -minimize EOT and increase of Cox => implementation of high-K(~20) ALD HfO_2

-reduce defects at high-K ox/ncSi & formation for plasma induced layer instead of native SiO_x => N_2 pretreatment before ALD + anneal for adhesion and interface species desorption

*Top gate: -minimize source/ top Al gate Loverlap => EBL3 design +alignment

*Metal S/D: less tunnel oxide consumption due to metal contact=> replacing Ti with TiN S/D sputtering + annealing for better contact resistance and ohmic contact

* Minimize parasitic capacitances (Cgs, Cgd, Cp) (MIM) to enhance switching frequency (f_c)

Semi-quantitative aspects

*Ion: (better channel mobility, less Dit , optimized strain, lower barrier/contact resistance, better tunnel)

Based on coulomb diamond measurements and comsol simulation, replacing the lateral/back gates previously adopted with 86nm SiO_2 as gate dielectric by a top gate with thinner gate dielectric <50nm or high-K) will allow an increase of gate swing (Î±) up to 30 V corresponding to an enhancement of I on current up to 100Î¼A/ Î¼m and Ion/Ioff in the range of 10^6 [2].

*Ioff: We need to maintain I off range or slightly improve it with minimizing Ntrap or adopt slightly longer channel (> 100nm)

*S. S: (Small EOT~5nm , higher Cox , reduced gate overlap , better interfaces) An increase of gate stack capacitance Cg allows better gate modulation at low Vgs, high carriers density in the channel, leading to high performance and low power consumption. The gate dielectric capacitance is described as follow whereas the equivalent oxide thickness for high-K dielectric is expressed as. As an estimation an expression for subthreshold swing parameter is given as:

Replacing the 86nm SiO_2 (K= 3. 9) by a 20nm HfO_2 (K~20) as gate dielectric, leads to a EOT= 4. 87 and an increase of C_{ox} by a factor (~x18). Thus, S. S can reach 250mV/dec.

Comparaison a-Si PECVD vs. a-Si LPCVD At 3IT, chemical deposition techniques, mainly LPCVD and PECVD are employed for silicon thin layer growth. It is important for our project to distinguish the relevant film properties, as well as, the implication on device performance for each technique.

Electrical Properties

In general, amorphous silicon thin films deposited by PECVD at low temperature (200-300°C) are disordered with a defect density in the range of 10^{18} cm^{-3} and hopping based conduction mechanism. The resulting film are usually under stress due to high deposition rate and ion bombardment. Whereas, LPCVD films deposited at relatively high temperature (~600°C) are more ordered with a lower defect density of about 10^{15} cm^{-3} and activation conduction mechanism [4]. Due to high temperature and low deposition rate a relaxation occurs in the film leading to low strain effect. Low field mobility of about 0. 1-1cm^{2} V^{-1} S^{-1} in such amorphous material is mainly attributed to punctual defects such dangling bonds and dislocations. Different other allotropic varieties are of interest for our channel mainly polycrystalline and nanocrystalline silicon can be obtained depending on process parameters. On one hand, poly-Si consists on a network of crystalline grains randomly oriented and separated by grains boundaries which are regions with high defects and dangling bonds concentrations. On the other hand, nc-Si film are formed by crystalline grains of nanoscale size (~ 50 nm-diameter) incorporated in an amorphous matrix with a grain crystalline fraction of up to 60% [5]. These changes in crystalline phase and microstructure imply a significant enhancement in field mobility from 50 up to 300cm^{2} variation of film microstructure along depth can be manifested, where the interface (nucleation phase) is formed a dominant amorphous phase or very small grains, but, as the growth evolves and the film becomes thicker, the size of the grains increases [6]. This difference in structure between the interface and the bulk of the film may have implications on electrical conduction, since carriers moving through amorphous phases, result in low mobility, whereas,

the transport through the large grain give rise to high mobility (figure III. 1) For our ncSi channel thin film(<50nm) deposited on SiO_2 , we anticipate low mobility range where an homogenous transport occurs through an amorphous interface with very narrow and similar grain sizes (green box).

Impact on device performances

In similar case to our ncSi channel, it was demonstrated, that the main origins of mobility degradation in poly-Si channel are Coulomb scattering due to defects inside the grain (D_{it}) -point defects or dislocations- or defects at the grain boundaries (Ntrap), as well as the surface roughness at the ncSi / gate oxide interface (Nit). On the one hand, defects inside the grains as the dominant limiting factor on electrons mobility control the on-current (Ion) value. On the other hand, defects at the grain boundaries (Ntrap) generate a Trap-Assisted Tunneling (TAT) mechanism in the (ncSi) channel, which degrades the off-current (Ioff) and the value of (S. S). Moreover, the traps at the interface (Nit) reduce the control of the grid which strongly affects (S. S) and (Ion) [7].