Computer organization

System software was introduced in the third generation of computers. A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (PIPS). Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. A number of chips can be grouped together to form a memory bank A characteristic of ROOM is that it is volatile. It is not necessary for the ALL to signal when overflow occurs.

Addition and subtraction can be performed on numbers in twos complement notation by treating them as unsigned integers. It has become common practice to use a symbolic representation of machine instructions. Addresses are a form of data. In a system without virtual memory, the effective address is a virtual address or a register. Register indirect addressing uses the same number of memory references as indirect addressing. The memory transfer rate has kept up with increases in processor speed. The control unit (CUE) does the actual computation or processing of data.

The processor needs to store instructions and data temporarily while an instruction is being executed. It is possible to improve pipeline performance by automatically rearranging instructions within a program so that branch instructions occur later than actually desired. The execution of a program consists of the sequential execution of instructions. The execute cycle is simple and predictable. It is important to design compact, time-efficient techniques for microinstruction branching. It is easier to design in hardware than in firmware. Short answer? App) a. The major structural components of the CPU are: control unit, register, CPU interconnection, and (ALIAS) b. A

more devices. Bus c. A . Arithmetic and logic unit is a communication pathway connecting two or interrupt simply means that the processor can and will ignore that interrupt request signal. Disabled RAM is made with cells that store data as charge on capacitors. Dynamic e. The simplest of the error-correcting codes is the code. Hamming f. The is that part of the computer that actually performs arithmetic and logical operations on data. G. Occurs when an arithmetic operation results in an absolute value greater than can be expressed with an exponent of 128. Overflow h. The operation of the processor is determined by the instructions it executes, referred to as or computer instructions. Aching instructions are bits in special registers that may be set by certain operations and used in conditional branch instructions. Status flags j. Source and result operands can be in one of four areas: main or virtual memory, immediate, 1/0 device, and k. The simplest form of addressing is . Processor register addressing. Immediate l. Just as register addressing is analogous to direct addressing, addressing is analogous to indirect addressing. Register indirect m. A processor must: fetch instruction, interpret instruction, process data, write data, and . Fetch data Occurs when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution. Pipeline hazard o. Data are exchanged with the processor from external memory through a p. The . Data bus register contains the value to be stored in memory or the last value read from memory. Memory buffer (MBA) q.

Control unit implementation techniques fall into two categories: microprogramming implementation and hardwired implementation. Processors, with their simpler instruction format, typically use hardwired

control units. RISC s. An alternative too hardwired control unit is a intro unit in which the logic of the control unit is specified by a micrograms. Microprogramming t. Each microinstruction cycle is made up of two parts: fetch and 3. Multiple Choice ? (App) a. Architectural attributes include x 1/0 mechanisms control signals interfaces memory technology used . Execute b.

The system bus main memory control unit c. The stores data. Interprets the instructions in memory and causes them to be arithmetic and logic unit d. During the the opposed of the next instruction is loaded into the IR and the address portion is loaded into the MAR. Execute cycle clock cycle instruction cycle etch cycle e. The data lines provide a path for moving data among system modules and are collectively called the address bus data bus -127 . Control bus f. Positive numbers less than 2 are called positive underflow positive overflow negative underflow negative overflow g.

Moving the sign bit to the new leftmost position and filling in with copies of the sign bit is called partial extension range extension sign extension . Bit extension h. Is when the result may be larger than can be held in the word size being used. X Arithmetic shift Overflow Partial product Underflow I. In the ARM architecture only processing tutus register access load and store branch instructions access memory locations. Data j. A branch instruction in which the branch is always taken is unconditional branch jump bi-Indian k.

For the immediate base register displacement mode, the operand is included in the instruction. X has the advantage of large address space, however it has the disadvantage of multiple memory references. Stack addressing Direct addressing Immediate addressing Indirect addressing m. The

advantages of addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required. Erect indirect n. The fetch decode execute write back o. The stage includes ALL operations, cache access, and register update. Oration of the control unit issues a repetitive sequence of pulses. Instruction register flag control bus signals clock MAR MBA holds the address of the next instruction to be fetched. X q. The groupings of micro-operations must follow which rule? A sequence of events does not need to be followed conflicts must be avoided in one time unit all of the above path r. Machine cycles are defined to be equivalent to bus s. Which of the following is a control unit input? . The set of microinstructions is stored in the control memory control address register.