Foundations of it-designing a computer architecture

Technology, Information Technology

Designing a Computer Architecture Current processors make use of a fast accessed cache memory that keeps data that are used somuch. The cache memory is little and, because it is quicker than the main memory, there is an apparent performance development (Von & Kurzweil, 2012). To perk up performance more, the processor core can posses a separate cache for data along with another for instructions. For instance, the Intel Pentium Processor N3500-series has a 32 KB L1 instructor cache as well as a 24 KB L1 data cache. Both are set up on the processor die.

For my Ideal computer, I would have the following specifications

1. A CPU of Intel 4th gen core i5-4200M (2. 5GHz, 3M cache)
2. A system RAM of 4GB and above
3. A hard drive of 320 GB Hard Drive at 7200 RPMs or an SSD/Hybrid
4. Removable storage 8X (DVD+/-RW) Drive
5. Monitor 1366x768 Min. Resolution
6. Video card Intel, NVIDIA Graphics or AMD, 1GB GDDR5 RAM

I would like my ideal computer to help me in research related to scientific computing. This will help me to develop and evaluate computer algorithms intended for simulating mathematical models of scientific trends. This area entails core problems in continuous algorithms like fast methods for handling linear algebra as well as solving differential equations. I will also build software for simulating challenging physical problems like turbulence in fluids along with crack propagation in solid materials. The computer will help me build accurate methods for discretizing continuous models even as it preserves physical invariants. In addition, I will carry out optimal estimation in the face of limited information.

At the moment, computers are based on the von Neumann architecture. Nonetheless, the von Neumann architecture has its limitations. In order to access the data and program in the memory, the central processing unit (CPU) had one bus. This is called the von Neumann bottleneck, due to the limited data transfer rate between memory and CPU. With just one bus, the data and instructions are accessed in sequence, so the CPU waits until the data loads from memory prior to executing the instruction. With the increase of CPU speed, it was evident that a solution is needed to defeat the bottleneck (" Von Neumann Architecture," n. d.).

These problems are connected to the von Neumann architecture. In order to overcome the von Neumann bottleneck, the stack memory is used. The stack is a particular memory region that is competently managed by the CPU. It is used to store up variables employed by functions. As a program calls a function, the function variables are pushed onto the stack. The access of variables is faster on the stack than when they were in the main memory, amounting to better performance.

Standing on the doorstep of the fifth generation, we obviously expect a lot from future computers than more speed. Computers have come this far in terms of enhancements to the current architectures and their accomplishment. The use of cheaper, smaller, and faster components is joined with better and superior parallelism. The hardest task associated with adopting new architectures is that it is difficult to think about them utilizing the von Neumann leaning minds.

References

The Von Neumann Architecture. (n. d.). Retrieved from http://www.

programming. msjc. edu/asm/Unit2/TheVonNeumannArchitecture. aspx

Von, N. J., & Kurzweil, R. (2012). The computer & the brain.