Adder subtractor research paper essay sample

Technology, Computer

Adder/Subtractor Research Paper Essay Sample

Full Adder is a combinational circuit that performs the arithmetic sum of three input bits. It consists of three inputs and two outputs. Three of the input variables can be defined as A, B, Cin and the two output variables can be defined as S, Cout.

The two input variables A and B represents the two significant bits to be added. The third input Cin represents the carry bit. We have to use two digits because the arithmetic sum of the three binary digits needs two digits. The two outputs represents S for sum and Cout for carry.

For designing a full adder circuit, two half adder circuits and an OR gate is required. It is the simplest way to design a full adder circuit. For this two XOR gates, two AND gates, one OR gate is required.

Circuit Diagram for the Full Adder

S= Cin XOR (A XOR B)

Cout= Cin(AB'+A'B)+AB

Half-Subtractor is a combinational circuit that subtracts two bits and produces their differences. It also has an output to specify if a 1 has been borrowed. Suppose the minuend bit is x and the subtrahend bit is y. If we want to perform x-y, we have to check the relative magnitude between x and y.

If x> y, we have three possibilities: 0-0= 0, 1-0= 1 and 1-1= 0. The result is known as difference bit. If x