

Abstract exceptional systems can be designed. risc

[Design](#), [Architecture](#)



Abstract - Therapid advancement of the microprocessor in our everyday life has bothsimplified and complicated.

Most of the people know that a microprocessor isresiding somewhere inside the computer, but what a microprocessor is and whatit does, remains a mystery. Microprocessor is a programmable electronic devicewhich is used in small system such a processors used for packet transmission, pocketcalculator, digital watches, smart telephone, personal computer etc. This paper describes study of 32-Bit RISCProcessor Using VHDL.

It uses four different format R-format, I-format, J-format and I/O format and eight 32-bit general-purpose registers. Theinstruction format used in this is based on MIPS RISC (ReducedInstruction Set Computer) Processor but the design process is simplewhich involves instruction fetch (IF), instruction decoder (ID), execution(EXE), data memory (MEM) and write back (WB) modules of 32-bit CPU. All the modules in this design arecoded in VHDL language, as this language is very useful to cope successfully with the parallelism of digitalhardware. The top-level module connects all the stages into a higherlevel.

For Simulation of the design XILINX14. 5i ISE Simulator is use.

I. INTRODUCTIONTheprocessor or Central Processing Unit (CPU) is the heart of the computer. It determines in a large part, howfast the computer will be and what capabilities the machine will have.

As the technology, hardware along withsoftware emerges, design alternatives also emerges. Furthermore, with theenhancement in designing processors, exceptional systems can be designed. RISCarchitecture is a

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reverberation to the developing technology and the accumulation of philosophy from the CISC designs. CISC processors were designed to simplify compilers and to improve performance under constraints such as small and slower memories. The outstanding appearance of Reduced Instruction Set Computer (RISC) are they accommodate simple yet efficacious set of instruction that can execute in single clock cycle, Register-to-Register Operations, load and store operations are used to access memory, Simple Addressing Modes, Large Number of Registers, uses the Harvard architecture, pipeline is easy due to the fixed length instruction. Most of the processors available now days have a pipelined architecture. The pipelined processors are designed in a way that they can process more than one instruction in the same clock pulse.

To achieve this phenomenon of multiple processing, the processors are designed to have multiple stages. These stages work together as single unit under common clock pulse to generate the effect of multiple processing. Generally we have Instruction fetch, Instruction Decode, Execution, Memory and Write back stages in a five stage pipelined RISC processor. Each of these stages works as a sub processor connected in the sequence. Such that with every clock pulse each of them process one instruction and forwards it to the next stage in the sequence. In this project, the simulation of a 32 bit MIPS RISC processor based on floating point concept will be done by using VHDL.

MIPS are the abbreviation for Million Instructions Per Second. This 32-bit processor design using VHDL (Very High Speed Integrated Circuit

HardwareDescription Language) mainly consists of eight 32-bit General PurposeRegisters, 32-bit Flag Register, A Control Unit, an Arithmetic Logic Unit (ALU), Decoder and Execution Unit and Memory Unit. This processor has fixed-length of32-bit instructions based on four different format R-format, I-format, J-formatand I/O format and eight 32-bit general-purpose registers. Thisprocessor used floating point IEEE 754 Standard format for ALU operation

II. ARCHITECTURE OF32-Bit PROCESSOR Our 32-Bitprocessor consists of following main blocks: 1. 32-Bit ALU2.

Decoder and Execution Unit3. Control Unit4. Register unitFig1. Block diagram of 32-Bit processor1.

32-Bit ALU: In32-Bit processor, ALU is of 32-Bit which can perform different arithmetic andlogical operation on maximum 32-Bit number at a time. The different arithmeticoperation is addition, subtraction, multiplication, division, increment, decrement etc. The different logical operation is ANDing, ORing, EX-ORing, complement etc. While ALU perform any operation either arithmetic or logicalthe 32-Bit result will be store into Result to Destination Unit.

2. Decoder and Execution Unit: Decoderperforms the function of instruction register and instruction decoder. Instruction register is a 32-Bit register which is used to store 32-Bit opcode.

During execution of program processor will fetch the opcode from program memoryand store it in instruction register. From instruction register, this opcodewill be given as an input to instruction decoder. Depending upon the

input to instruction decoder, one of the decoder output become active and corresponding instructional circuit available at that active output. 3.

Control Unit: The function of control unit to generate the control signal at that active output and the signals are given to all those blocks which are involved in that operation to complete the operation.

4. Register Unit: Register unit consist of four main registers. They are as follows: a. Registers: It is a 32-Bit register which is used to store 32-Bit data or 32-Bit result temporary while performing any arithmetic or logical operation. b.

Flag Register: In 32-Bit processor, flag register is of 32-Bit which consists of 32 flip-flops. Flag register is used to indicate the status of result obtained in Result and Destination Unit. c. Program Counter: Program counter is a 32-Bit register, which is used to store 32-Bit address of that memory location from where program opcode is to be fetched. After every opcode read operation, PC will be auto increment by one.

So that next time next opcode will be read or fetch. Thus PC can also be defined as 32-Bit register which hold 32-Bit address of next memory location from where next opcode is to be fetched or read. d.

Stack Pointer: Stack pointer is of 32-Bit which is used to store 32-Bit address of stack top memory location in internal RAM or data memory. During PUSH operation SP will be auto increment by one.

III. METHODOLOGY

Fig 2. Overview of processor

IV. INSTRUCTION FORMATS The MIPS architecture of RISC Processor is

based on four Instruction formats R-Type, I-Type, J-Type and I/O Type illustrated in the Fig below: Fig3.

MIPS instruction format with a new type a) R-Type (Register Format) In this format 32 bits are divided into six fields. Bit number 31 and 30 are used to select the type of Instruction format, opcode is of 6 bit which are used to select the type of operation which is to be performed. Source register (Rs), Target register (Rt) and Destination register (Rd) are of 5 bit each which are used to store the data on which operation is to be performed and also store the result. Shift amount (shamt) is used to store the shift amount by which the data is to be shifted. Function field is of 6 bits and is used to select the variant of opcode (function code). b) I-Type (Immediate Format) In this format there are total four fields, bit number 31 and 30 are used to select the type of Instruction format, opcode is of 6 bits which is used to select the type of operation which is to be performed.

Two registers are used in this type of instruction, source register (Rs) and destination registers (Rd) which are of 5 bits each. The remaining bits are used to give the address of immediate value on which operation is to be performed. c) J-Type (Jump/Branch Format) In this format there are only two fields, Instruction format selection bits are 31 and 30 bit, opcode is of 6 bits which is used to select the type of operation which is to be performed. Target address is of 26 bit which specifies the address on which it needs to be jump or branch. d) I/O-Type (Input/Output Format) In this format there are total four fields, all the fields are similar to R-Type and I-Type formats. The bit number 31 and 30 used to select the type of Instruction format,

opcode is of 6 bit which is used to select the type of operation. Source register (Rs), Destination register (Rd) are used in this type of format.

These types of instructions are used for reading and writing port data. The selection of type of instruction on basis of opcode bits are as follows:

SR NO.	OPCODE TYPE OF INSTRUCTION	BIT 31	BIT 30	1	0	0	Register Type	2	0	1
1	Immediate Type	3	1	0	Jump/Branch type	4	1	1	Input/output type	Table no.

1 Because of these four formats, execution of any instruction becomes faster, hence the proposed processor is also called as High Performance Processor.

V. APPLICATION Personal computers, Laptops etc.

Cell phones As a practical kit for student Robotics Game Consoles This processor can be use for packet transmission.

VI. CONCLUSION The availability of low cost, low power and small weight, computing capability makes it useful in different applications. IEEE 754 BASED SINGLE PRECISION MIPS RISC processors have high performance and less power than 32 bit processors without MIPS. VHDL is also a very useful hardware description language. It is a very powerful language with numerous language having capability of describing very complex behavior.

The CPU is described by a number of lower-level components that are instantiated to form the CPU design. In this work IEEE 754 BASED SINGLE PRECISION MIPS RISC processors is design with reduced power. The main aim of this project is to increase frequency and relatively time is less.