Digital intermediate frequency in lte superheterodyne

Research and implementation of the digital intermediate frequency in LTE superheterodyne transmitter

Abstract:

Digital IF (Intermediate Frequency) is an indispensable key technology in modern communication, among which digital up converter (DUC) and digital down converter (DDC) are important parts between baseband and IF. In this paper, we give a general method and solution of designing digital IF to meet the demands of practical application. Firstly, we analyze the theories and technologies of digital IF including filter bank and DUC. Secondly, we set about analyzing how to design filter bank in key part and implement a superheterodyne. Finally, we put forward a specific design plan of DUC and develop a digital IF suitable for TDD-LTE (Time Division Long Term Evolution) system. The results of simulation show that our design method of DUC can satisfy the requirements of relevant indicators. It has been implemented on FPGA platform in a practical LTE based transmitter.

SECTION I. Introduction

Nowadays, digital subscriber line (DSL) network far remains one of the most promising means of broadband communications. DSL communication is evolved from conventional discrete multitone (DMT) system to filtered architectures. The smooth evolution of filtered multitone, FMT, provides higher peak rate and higher spectrum efficiency as the widening of the limited frequency increases.

As the frequency resources become increasingly scarce, research on subband coding in the field of high-speed DSL communication is of great significance. Adaptive subband estimate is the core of the FMT receiver. With the development of FMT technology, an orthogonal filter bank transmissions have become the focus of attention.

As the key technology of recent multirate systems, filter banks technology is also the starting point to a breakthrough of frequency selective transmissions.

For frequency selective channels, digital up-conversion must be completed firstly before filtering. Analysis filter bank structure mainly includes filtering, interpolating, mixing and resampling. Filter bank implementation involves the computation of an efficient spectral allocation and often estimates high complexities. It is very difficult to implement full corresponding spectral after sampling using the current DMT [2]. In application design, the common method is to use DMT in the time-domain to achieve digital up-conversion. In this paper, we mainly research the theoretical characteristics of the digital up-conversion in the frequency-domain, and design a set of digital up-conversion scheme suitable for FMT system. Finally, the design of subband transmissions is implemented.

SECTION II. Design Requirements of DUC

DUC usually needs spectrum shifting that modulate the baseband signal to band-pass signal.

Because of the lower sampling rate of baseband signal, it cannot meet the needs of radio-frequency emission.

The sampling rate conversion should be added.

The method to implement DUC is as follows.

At first, the signal is divided into two channels baseband signal (I, Q).

Then the signal is transformed into a higher sampling rate through the filter interpolation.

Finally the two-way signals are respectively modulated and thus the spectrum is moved to a specific point through the digital mixer.

Up-converter module is realized using filter bank cascade and finally modulate it to realize the spectrum shift.

The up-converter principle block diagram is shown in Fig. 1.

Figure 1

Figure 1.

The up-converter principle block diagram.

View All

Usually, the sampling rate can be improved through the filtering and interpolation [3]. We modulate the baseband signal to the NCO (Numerically Controlled Oscillator) intermediate frequency carrier. This paper designs a

broadband wireless DUC which is operated based on the TDD-LTE standard and the bandwidth is 5MHz. The Third-Generation Partnership Project (3GPP) standards specifies that the sampling rate of signal carrier 5MHz bandwidth TDD-LTE is 7. 68Msps. In order to shift the spectrum to the intermediate frequency 21. 4MHz, signal needs to use interpolation for 8 times to achieve the sampling rate up to 6I. 44Msps. Then we make analog transformation in DAC according to the Nyquist sampling theorem. DUC provides the function of spectrum shaping and improving the sampling rate, with the premise of satisfying the requirements of 3GPP standards. In 3GPP TS 36. 804, it puts forward the specific spectrum requirements to the front-end of digital transmitter. On the one hand, the suppression performance outside the band of filter needs to meet the regulation of the spectrum template [4], [5]. On the other hand, it needs to satisfy the requirement of the 5MHz broadband. In addition, the sampling rate should be increased 8 times. The specific indicators is shown in Table 1.

Table I. Design requirements of DUC

Table I.

SECTION III. Detailed Design Scheme of DUC

In this paper, the multi-stage interpolation is adopted in DUC part. The total design is shown as Fig. 2:

Figure 2

Figure 2.

Digital up converter design.

View All

We need 8 times interpolation, therefore the design uses two CIC filters of 2-fold interpolation. Because the interpolation factor is a power of 2 times, particularly suitable for Half-band filter, we cascade a Half-band filter to achieve interpolation filtering function.

A. Interpolation Theory

Interpolation [6] is an integer multiple insertion of the original sequence. We do I times interpolation by inserting (I-1) zeroes between the adjacent two sampling points. The relationship between original sequence x(n) and interpolated sequence xI(n) is shown as:

xI(n)={x(nI), 0, nI is integerothers(1)

View SourceRight-click on figure for MathML and additional features.

Spectrum relationship is obtained as:

XI(ejω)= X(ejωI)(2)

View SourceRight-click on figure for MathML and additional features.

The original sequence does I-fold interpolation in the time domain, which is I times compression for the original spectrum. General interpolation method is inserting zeros between the sampling sequences. However, the signal spectrum XI(ejω) after interpolation not only contains the fundamental

frequency X(ejω), but also high frequency mirror, the frequency of which is greater than π/I. In order to recover the original signal spectrum from XI(ejω) we need to put signal through a low-pass filter with bandwidth π/I. After low pass filtering, the inserted zero point smoothly get into the accurate value of x(n).

Figure 3

Figure 3.

Signal and spectrum before and after interpolation.

View All

The maximum output frequency of interpolation can reach (I-1) times of which of original sequences. The frequency spectrum of the signal is consistent with the original spectrum but frequency shifts, as is shown in Fig. 3.

When the sampling rate is transformed, the I times interpolation can be realized by using only single stage. But if we design a low pass filter with larger interpolation multiple factor using the same method of single stage, the order of the transfer function h(n) will be relatively high. It’s difficult to implement on an embedded hardware for its large requirement of storage and calculation. So in order to implement easier and reduce calculation, this paper uses a method of multi-stage interpolation and cascaded together [7]. A simple two-stage interpolation method is shown as follow Fig. 4:

Figure 4

Figure 4.

Multi-level implementation of interpolation(i= i1*12).

View All

After processing by multi-stage method, the order of the interpolation filter is decreased obviously.

B. CIC Filter Principle and Design

CIC (Cascade Integrator Comb) filter, a kind of efficient extraction or interpolation filter, is been widely used in the multi-rate signal processing. The basic components of CIC filter include two parts: integral and comb filtering. Single-stage CIC decimation and interpolation filter is shown in Fig. 5. Where, M is latency state, D is extraction factor and L is interpolation factor.

Figure 5

Figure 5.

CIC decimation and interpolation filter structure.

View All

In single-stage decimation CIC filter, the integrator stages N= 1, and the feedback coefficient is 1: The state equation is defined as:

$$y(n)= y(n-1)+x(n) \quad (3)$$

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From (3) we can obtain the Z transform as:

HI(Z)= 11−Z−1(4)

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The state equation of comb section is defined as:

y(n)= x(n−1)−x(n−DM)(5)

View SourceRight-click on figure for MathML and additional features. where M is state delay, its function of Z transform is as:

HC(Z)= 1−Z−DM(6)

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Transfer function of extraction CIC filter is defined as:

H(z)= HI(Z)HC(Z)= 11−Z−1(1−Z−DM)(7)

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From (7) we can obtain its frequency response as:

H(ejω)= sin(ωDM/2)sin(ω/2)(8)

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The amplitude-frequency characteristics of single-stage CIC filter has a higher sidelobe, so we can use a multi-stage cascade CIC filter to reduce

sidelobe and improve stop-band attenuation. The system function of CIC filter can be expressed as:

H(z)= HNI(Z)HNI(Z)=(11−Z−1)N(1−Z−DM)N=[∑D−1K= 0Z−k]N(9)

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When we set CIC filter’s order D to the multiple factor of interpolation I and do an equivalent transformation, the CIC interpolation filter cascading in practical applications will be shown as Fig. 6:

Figure 6

Figure 6.

Cascading structure of CIC interpolation filter.

View All

Considering the system requirements and debugging repeatedly by MATLAB, we set the design with stages N= 2, sampling rate R= 3 and delay M= 1. Then we can get the frequency response of interpolation CIC filter with the parameters N= 5, M= 1, R= 3, as shown in Fig. 7:

Figure 7

Figure 7.

Frequency response of CIC filter after 2x interpolation.

View All

C. CIC Compensation Filter Design

CIC filter has good anti-imaging and anti-aliasing effects. In the design of the decimation/interpolation filter, it is indispensable to get a relatively flat pass-band and a relatively narrow transition band especially for broadband systems. Consequently, if the CIC is applied to the broadband systems, the pre-compensation and compensation filter which can significantly improve the performance of the filter is needed.

The amplitude response of the compensation filter is the reciprocal of the CIC filter in ideal circumstances. When we use an equal-ripple FIR [8] filter with anti-sinc function as the CIC compensation filter, its spectrum after two filters cascade will be shown as Fig. 8.

According to the requirements of 5MHz bandwidth of our special TDD-LTE system, we set the parameters of CIC filter as fellow: cutoff frequency of pass-band B= 5MHz, interpolating multiple D= 2 and input sample rate is 30. 72MHz.

Figure 8

Figure 8.

CIC and CIC compensation filter cascade effect.

View All

The so-called compensation means cascading a compensation filter in front of the filter bank. After simulation cascade in MATLAB, the band ripple of CIC

filter is shown in Fig. 8(b). As can be seen from the figure, the band ripple drops about 3dB. After compensation filter processing, we find the attenuation of pass-band ripple improves so significantly that it can meet the design requirements.

D. Half-Band Filter Design

Half-band filter is a pretty useful and special filter and it plays an important role in the high speed signal processing and multi-stage filter design. Half-band filter is also a kind of FIR filter, and its impulse response h(k) is even symmetry with respect to the coordinate axis with the character of h(k)= h(-k).

h(k)={1, 0, k= 0k=±2,±4(10)

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According to the above formula, we learn that the impulse response of Half-band filter is not 0 except in the coordinate zero point but the rest of even position is 0. This feature is very suitable for achieving the decimation and interpolation of power of 2 times. When using Half-band filter for sample rate conversion, the system can save half amount of calculation.

Therefore, Half-band filter cascade is widely used in high order filter design and high-speed processing.

For Half-band filter, Stop-band bandwidth π−ωA is equal to pass bandwidth ωc, and the width of the transition zone is determined by the pass bandwidth

and sample rate together by consensus. In addition, the pass-band and stop-band ripple is the same. As is shown in Fig. 9:

Figure 9

Figure 9.

Half-band filter.

View All

As we can see from above figure, the response of Half-band filter in $\pi/2-\omega A$ interval is not zero. When making 2 times extraction, it does not satisfy the conditions of extraction without aliasing, which will result in signal aliasing distortion. But the spectral structure of signal ($0\sim\omega c$) in the pass-band has not been damaged and it can still be recovered without aliasing, so we can still use Half-band filter to design 2-times sample rate conversion of pass-band signal. In DUC design of this paper, we cascade a Half-band filter to achieve 2-times interpolation.

After completing the design of filter banks, we simulate the solution in MATLAB and the result is shown in Fig. 10:

Figure 10

Figure 10.

Frequency response of our filter bank.

View All

SECTION IV. Simulation Results

A typical TDD-LTE signal with 5MHz bandwidth is shown in Fig. 11. The baseband signal at the zero frequency is moved to 21. 4MHz after up-converter.

Figure 11

Figure 11.

Signal spectrum before and after up-converter.

View All

As can be seen from the figure above, the design of our program meets the design requirements. Specially, in Fig. 11(a) we add two noise signal outside the passband into input signal. After the designed filter banks, the additional noise signal is also normally filtered out and the indicators such as band attenuation and ripple all meet the requirements. It is shown in Fig. 11(b)-(c).

SECTION V. Implementation on FPGA

At the end of design, Xilinx’s xc7a200t-3fbg676 chip is selected to implement the system using VHDL language [9]. Simulating and synthesizing processes run in Xilinx [10] ISE14. 3 development environment. The specific implementation structure is shown in Fig. 12. There are mainly five parts: 1) DUC_pre_tx (stabilizing date rate of the up-converter input data to ensure a constant rate for the next module); 2) CIC _ compensation (compensation filter of CIC filter which has a certain filtering characteristic); 3) CIC filter

(achieving the function of filtering and interpolation); 4) halfband (achieving the function of filtering and interpolation); 5) dds_modulate_tx (moving spectrum from zero frequency to IF 21. 4MHz).

Figure 12

Figure 12.

Realization diagram of fpga.

View All

Fig. 13 shows the signal waveform after interpolation with CIC compensation module in simulation tool ModelSim. As can be seen from the figure, the input signal is filtered as expected. The original signal is mixed with high-frequency signal and the high-frequency part is filtered through CIC filter compensation. It indicates that our filter design has reached satisfactory results.

The signal waveform processed by CIC and halfband filter is shown in Fig. 14. We can see from figure that the original input signal becomes smooth, which suggests that the signal processing is successful.

The signal waveform processed by dds _ modulate _ tx module spectrum shifting is shown in Fig. 15. In the figure, we can see that the signal spectrum has been moved successfully from baseband to intermediate frequency.

Figure 13

Figure 13.

Waveform and spectrum before and after interpolation.

View All

Figure 14

Figure 14.

Waveform after CIC and half-band filter.

View All

Figure 15

Figure 15.

Waveform and spectrum after frequency shifting.

View All

SECTION VI. Conclusion

This paper introduces a general design method for digital IF and analyzes the main parameters that affect its performance. According to the specific index of TDD-LTE, we calculate the values of various parameters that the system needs. In addition, we analyze the frequency spectrum, band-pass ripple and band-stop ripple to judge whether they meet the requirements. The designs of CIC filter and Half-band filter are analyzed respectively. After that we analyze and design a CIC filter compensation best with the purpose of achieving possible to meet the system design requirements. Finally, we verify the actual effect of the filter in Model and implement the design on

FPGA platform. The result suggests that the design method is reasonable and feasible.