

Low power ptl based arithmetic leaf cell engineering essay

[Engineering](#)



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Engineering Chennai, India – 600119. Email: reeba26in@gmail. com Abstract

—Though the technology hunt is on for sub - 10nm, the circuit level abstraction is still proving as the eminent way to reduce power in any form of digital design. In this work, one bit full adder cell is implemented using the pass transistor method as an arithmetic leaf cell. The CCMOS, BBL-PT, ULPGA, SERF and Transmission Gate Logic styles are taken for comparison. The results show that the proposed design operates at low power than the other methods which are compared. The power consumed by the new 13T adder as a leaf cell is 33 times less as the maximum optimization when compared to BBL-PT adder. Index Terms—13T adder, low power, PTL adder, 1bit CCMOS adder, power efficient, arithmetic leaf cell.

Introduction

Minimizing power, delay and area are the important constraints in all kind of digital VLSI design. But all the factors are impossible to meet in parallel. The growing global population demands the need for productivity of gadgets which are to be handy and cheaper. The device scaling is the key technique for miniaturization of such digital equipments. There are many advantages of scaling for low-power operation. The improved device characteristic for low-voltage operation is one of them. This is due to the improvement of the current driving capabilities. Improved interconnect technology is used to minimize the parasitic effects. Reduced junction capacitance is another

result of scaling the device. Availability of multiple and variable threshold devices lead to MTCMOS technology. This results in good management of active and standby power trade-off and higher density of integration. The sleep transistor and power gating are the familiar methods in connection with scaling the devices. However, as the size of CMOS circuits become smaller, high performance is more difficult to achieve due to the effect of velocity saturation [1] – [2]. At short channel lengths L , the drain current per channel width (W) is no longer proportional to $(V_{gs} - V_t)^2/L$, where V_{gs} is the gate-to-source voltage and V_t is the threshold voltage. The drain current is proportional to $V_{sat} \cdot (V_{gs} - V_t)$, where V_{sat} is the saturation velocity [3] – [4]. Moreover, at sub-micron level the difference between the operating voltage and threshold voltage is very small and the static leakage is dominant to increase the static power consumption. This situation increases the design complexity and careful design of the system becomes more dominant factor. However the technology scaling has already reached the saturation level. The current scenario looks ahead the alternate solution to the VLSI industry to keep the Moore's law to be true. Power optimization with a satisfied delay and area or vice-versa can be achieved with the help of various abstraction levels. Out of such abstraction levels, the circuit level approach is the competent one to reduce the power despite thinking the technology scaling alone. Though the circuit approach seems to be very complicated and more time consuming to design or re-engineer the desired modules, the throughput is good at the final stage. In general, the power dissipation in a CMOS circuit is expected to be smaller along with a minimum delay. Technology, circuit design style, architectural abstraction and algorithmic abstraction are

the factors which influence the power dissipation in CMOS circuit. CMOS circuit is robust as it is proven already due to its pull-up and pull-down networks which ensure the full swing and hence immune to noise factors. Numerous CMOS circuit design styles exist which are static and dynamic in nature. The following paragraphs brief the logic styles available to construct a 1-bit adder cell. The full adder employed with PMOS transistors to allow the output to be charged high and NMOS transistors to discharge the output node to ground, is of CMOS style. The PMOS pull-up networks are hence used to ensure the output to a full logic high level. The NMOS pull-down networks, on the other end are used to ensure the output to a full logic low level. All together, the CMOS circuit operates to produce a full swing output voltage. NO RAcE dynamic CMOS (NORA) is another method of constructing a full adder. The P-type stage which forms the carry output is dynamically pre-charged high while the N-type tree which computes the sum is pre-discharged to ground. This process requires a two phase clock. Cascode voltage switch logic (CSVL) is another method to design a full adder. It is a dynamic logic family like a NORA. But it never requires a complementary clock. Another alternative method to the CMOS static complementary logic is the conventional pass-transistor logic based on MOS switches. It consists of a complementary pair connected in parallel. It acts as a switch, with the logic variable A as the control input. If A is low, the gate is OFF and presents high resistance between the terminals. If A is high, the gate is ON and acts as a switch with an on resistance of R_{on} . The literature review on a 1-bit full adder cell is given in section II along with the other adder methods which are considered for this work. The implementation of the proposed – new 13T

adder is to be given in section III. The simulation and performance comparison in terms of average power and delay are available in section IV. The work is concluded in section V.

Previous 1-bit Full Adders

In general, a one bit full adder has three 1-bit inputs A, B, and Cin which are required to calculate the two 1-bit outputs Sum and Cout. They are expressed as, $Sum = (A \oplus B) \oplus Cin$ (1) $Cout = A \cdot B + Cin \cdot (A \oplus B)$ (2) The selection of 1 bit adders for the comparison is based on the performance metrics of the methods which depend on power, delay and area. Another important factor is to consider the full swing output which yields a robust adder design. The module operates with lower switching activity consumes low power. The circuit with less number of nodes has the possibility of faster propagation. Among all such considerations, the design with less device count is also taken into account which leads to less chip area. Hence CCMOS, TFA, TGA, BBL-PT, ULPFA and SERF adder are taken for analyzing along with the proposed design due to the competency of these logic styles in terms of aforesaid factors.

Regular CMOS Adder

The Complementary static CMOS (CCMOS) adder is termed as regular adder which uses the PMOS pull-up and NMOS pull-down networks (complement to each other) with a minimum possible MOS transistors as in Fig. 1. The expressions to construct sum and carry are derived from (1), (2) as $S = A \oplus B \oplus Cin$ (3) $Co = A \cdot B + Cin \cdot (A \oplus B)$ (4) Where S is the Sum output and Co is the Carry output and the inputs with a single

punctuation (') are the complementary inputs. To reduce the device count, (3) is simplified as $S = AB' Cin + Co' (A+B+Cin)$ (5) Equation (5) is required to reduce the transistor count with the help of logic sharing between the sum and carry generation circuits [5]-[6]. This is also in other words useful to reduce power consumption due to reduced device count. Substituting (4) into (5), $S = AB' Cin + (AB + BCin + ACin)' (A+B+Cin)$ (6) $= AB' Cin + (AB)'(BCin)'(ACin)' (A+B+Cin) = AB' Cin + (A'+B')(B'+Cin')(A'+Cin')(A+B+Cin)$ Solving the expressions results in (3). Hence the logic equivalence can be easily verified. Though the logic sharing is used in the design, it still requires large area with 28 transistors. In the carry generation circuit, the signal propagates through two inverting stages. This leads to an increased delay in the carry path. Moreover it is an important factor to be carefully handled to keep it in control. The reason is that in an arithmetic circuit, the carry rippling to higher stages of a multiplier is the critical path [7].

Transmission Function Adder

The next method is the Transmission Function full Adder (TFA) which is as in Fig. 2. It consists of 16 transistors. The basic XOR circuit used in the design requires one of its two inputs in complementary forms. An additional inverter is thus needed, which leads to a 6-transistor XOR design. The design employs 4 CMOS transmission gates and can achieve full voltage swing operations and also operates at low power [8]-[10]. The main disadvantage of this logic styles is that it lacks the driving capability. When TFA is used in cascaded stages, its performance degrades significantly due to threshold voltage decay.

Transmission Gate Adder

The third logic design is denoted as TG-CMOS. It contains 20 transistors and uses only transmission gates and inverters to implement XOR and multiplexing functions. It is a widely used solution to deal with the voltage drop problem. NMOS transistor passes a strong 0 but a weak 1 and the PMOS does a strong 1 and pass a weak 0. CCMOS uses a PMOS pull up and an NMOS pull down whereas the transmission gate combines the best of both device advantages [11] – [14] by placing an NMOS device in parallel with a PMOS as in Fig. 3. The transmission gate acts as a bi-directional switch controlled by gate signal C as shown in Fig. 4(a). When $C = 1$, both inputs are driven, allowing the signal to pass through the gate. It is expressed as, $A = B$ for $C = 1$. Otherwise the PMOS and NMOS are at cut-off state. To understand the function of a transmission gate, consider the charging node B to Vdd as in Fig. 4(b). Node A is set to Vdd and the transmission gate is enabled ($C = 1$ and $C' = 0$). Since both the NMOS & PMOS transistors are on, the node B is fully charged to Vdd. On the other hand, while discharging the node B to 0, B is initially at Vdd when the node A is driven low. The PMOS can pull-down the node B to VTP at which moment it turns off. The parallel NMOS device stays turned on and at $V_{GS} = V_{dd}$ the node B is pulled down to GND. Though the transmission gate needs two transistors to achieve this condition, it ensures a full swing.

BBL – PT Adder

This is a hybrid full adder which has the combination of Branch Based Logic and Pass Transistor circuits (BBL – PT). Low power consumption is the prime objective of this method. The circuit is implemented with a few transistors

and less intra-cell node connections as possible. Hence the structure is implemented using branch-based design technique which meets the requirements while ensuring robustness with respect to voltage and device scaling. Fig. 1. Regular CMOS full adder Fig. 2. TFA full adder (a) (b) Fig. 4. Functions of transmission gate: (a) Charging node B, (b) Discharging node B. Fig. 3. TGA full adder (a) (b) Fig. 5. BBL – PT full adder: (a) Sum circuit, (b) Carry circuit. At the physical design level, this branch-based design diminishes the diffusion capacitance since it eases diffusion-sharing which leads to regular and compact layout. Series connection of transistors between the output node and the supply rail forms the branch like circuit and hence the name BBL. Using Karnaugh's maps, the circuit is optimized with PMOS and NMOS networks to produce the sum of products of the Boolean expression. The carry block is constructed using branch based logic as in fig. 5(b). But the sum block doesn't follow this method of implementation, because it requires 24 transistors to construct. Pass transistor logic (PT) is used to achieve the functionality with less device count [15]. The sum block with the PT structure is hence computing the arithmetic function $AB + BC_{in} + AC_{in}$ which is shown in fig. 5(a). The one bit adder of this type is therefore termed as BBL-PT, because it uses the BBL method to compute carry and PT method to estimate the sum output.

ULPFA

It is an Ultra-Low Power Full Adder (ULPFA) which consists of Low Power (LP) XOR gate. The sum logic is achieved by connecting the PMOS and NMOS transistors in a way similar to complementary pass transistor style. Two PMOS transistors in series and 2 NMOS transistors arranged in a manner

along with an inverter forms a two input XOR gate. This arrangement is again replicated and connected with it to form the circuit of a three input XOR gate as shown in fig. 6. The circuit to compute the carry output signal is similar to the carry computation circuit given for a BBL-PT adder as in fig. 5(b). Fig. 6. Sum Circuit of ULPFAThis method operates at a supply voltage less than 1volt and hence the design is named as Ultra-Low Power Full Adder. It operates consistently even under the voltage less than 0. 6V as mentioned in [15]. Another benefit of this logic style is that the leakage power is negligible than the consumption by a MOSFET. But the delay of the sum circuit worsens at the supply voltage less than 0. 8V.

SERF

The other logic style which competitively consumes lower power is the Static Energy Recovery Full adder (SERF). In the Conventional CMOS, the load capacitance charged to V_{dd} is discharging to ground when the output is switching from logic ' 1' to logic ' 0'. This kind of non-energy recovery leads to higher short circuit power P_{sc} . Whereas in an energy recovery circuit, the charge stored at the load capacitor (CL) is recycled to the circuit and hence the energy recovery full adder is a power efficient design as represented in fig. 7. This idea leads to a full adder with less transistor count and tremendous decrease in total power utilization. Fig. 7. Static Energy Recovery Full adder (SERF)The SERF adder design needs only 10 transistors to construct the complete 1-bit adder logic unit which is the lowest among all the other styles described so far. Hence it leads to the requirement of lowest die area. The transient function of this kind of adder is faster and competent with the other logic methods taken for analysis. But it has the problem of

threshold loss, i. e., the circuit is producing the degraded output. The use of this type of adder hence becomes critical when it is used to build larger system.

NEW 13T – PTL ADDER

A. Pass Transistor Logic (PTL)

Conventionally the inputs are applied to gate terminals of transistors. In pass-transistor circuits, the inputs are also applied to source and or drain terminals. The Pass Transistor Logic is generally constructed with the help of NMOS alone or parallel combination of PMOS and NMOS as transmission gates. The transistors in such circuits are working as switches and are providing the control over the parts of entire circuit. Implementation of complex gates can be possible with minimum number of transistors which results in a simpler circuit and the node capacitance is also reduced [16]. Pass transistor is a ratio-less logic class. The dc characteristics are not affected by the size of transistor. Increasing the size reduces the resistance but this can be offset by the increase in diffusion capacitance. Pass transistors in a cascaded chain can be arranged from largest to smallest to reduce delay. The pass transistors have a series resistance associated with them.

B. Proposed 13T PTL design

Yet again there are enough chances available to optimize a digital VLSI design with circuit level abstraction. It is very hard to construct and re-engineer a design at this level. However, doing so carefully will surely yield new dimension to a circuit with optimized performance. The use of reduced

logic gates is possible in a circuit if there is an existence of logic sharing. Concurrently, there is a possibility of circuit construction with few transistors using the PTL method. Fig. 8 Proposed 13T - PTL Full Adder

The proposed method is constructed using the simple Boolean based full adder of PTL style. The following few paragraphs have the implementation strategy into two groups namely the sum circuit and the carry computation. In the Sum circuitry, input signals B and C are used to compute a two bit XOR function in the first half with merely two transistors. The node X is used to express it as, $X = B'C + BC'$ (8) On the other hand the node X' is offering an XNOR function which is produced with the help of an inverter at node X. This node is also used to restore the swing with the help of a static CMOS inverter. From (8), the XOR is inverted using CMOS inverter to get XNOR output expressed as, $X' = (B'C + BC')'$ (9) The sum output is the combination of an XOR and an XNOR with the conditions A= 0 and A= 1 respectively. Hence the output stage of the sum has two transistors with a total of six transistors which is expressed as $S = A'X + AX'$ (10) Using (8) and (9), $S = A'(B'C + BC') + A((B'C + BC')')$ (11) This is also expressed as, $S = ABC$ (12) To generate the carry, 7 transistors are needed. The first part of the carry has three transistors to give the functions of AND, OR logic gates. The next part is the output node which results in a carry output of 13T 1-bit full adder. At the node Y, $Y = A.B$ (13) At the node Z, $Z = B.C + A.C$ (14) At the Carry Output, the top most transistor yields Y. Z.'. The carry is expressed as, $Co = YZ' + Z$ (15) $= A.B(B.C + A.C)' + Z = A.B(C(A+B))' + Z = A.B(C' + (A'.B')) + Z = A.B.C' + A.B.(A'.B') + Z = C'(A.B) + 0 + Z$ Substituting Z from (14), $Co = C'.A.B + BC + AC$ (16) Simplifying, $Co = A.B + B.C + A.C$ (17) All the above two

output generations of sum and carry require a new and simple PTL design with only 13 transistors as in fig. 8. The outputs in terms of power, delay and PDP have been given in the next section.

EXPEIMENTAL RESULTS

The simulation is carried out with the use of Low Power – 90nm Berkeley Predictive Technology model for analyzing the discussed 1 bit adder cells. The circuits are simulated with a supply voltage of 1V. It is because of the performances of the various methods at this potential level are good. All the adders are simulated and performance measures are tabulated for the same test conditions. The length and width of PMOS and NMOS of the adders are kept uniformly like an unit sized inverter for this purpose. The following paragraphs describe and compare the average power consumption, propagation delay and power delay product of the methods being considered for comparison with the proposed 13T adder. In the table I, the average power consumption, Propagation delay and Power Delay Product (PDP) are shown for the seven methods. The average power is calculated for the whole adder of each method. But there are two propagation delay measurements per logic style which are tabulated. It is due to the difference in delay between sum logic circuit and carry path in each design style. Hence PDP also has two different values per style. Table I – Average Power, Delay and PDP

(V_{dd}= 1v)

Adder Type

CCMOSTFATGABBL-PTULPFASERF13T Average Power (μW) 1. 5625. 5123.

3748. 0532. 9231. 731. 43 Sum Delay (ns) 4. 90314. 93034. 93333. 62224.

93134. 98924. 9954 Carry Delay (ns) 6. 27084. 99984. 99984. 90915. 03895.

00649. 9866 PDP - Sum (fWS) 7. 65125. 77115. 29174. 04162. 34158. 317.

14 PDP - Carry (fWS) 9. 79127. 54116. 82235. 88165. 88158. 8514. 28(a)

(b) Fig. 9. Average power of the various adders Fig. 10. Propagation Delay: (a)

Sum-Delay (b) Carry-Delay (a) (b) Fig. 11. Power Delay Product (PDP: (a) Sum-

PDP (b) Carry-PDP Table – II Comparison of 13T adder with other Adder styles

in percentage Parameter Comparison with 13T Leaf Cell in percentage

(%) CCMOSTFATGABBL-PTULPFASERF Average Power 9 ↑ 18 X ↑ 16 X ↑ 33 X

↑ 23 X ↑ 22 X ↑ Sum-Delay 2 ↓ 1 ↓ 1 ↓ 27 ↓ 1 ↓ 0. 1 ↓ Carry-Delay 37 ↓ 50 ↓ 50

↓ 51 ↓ 49 ↓ 50 ↓ Sum-PDP 7 ↑ 18 X ↑ 16 X ↑ 24 X ↑ 22 X ↑ 22 X ↑ Carry-PDP 31

↓ 9 X ↑ 8 X ↑ 16 X ↑ 11 X ↑ 11 X ↑ Device Count 28T ↑ 16T ↑ 20T ↑ 18T ↑ 24T

↑ 10T ↑ Legends: ↑ - More than 13T, ↓ - Less than 13T, X - Multiple times The

average power consumed by the new 13T - PTL adder is less than the

utilization of power by the other methods taken for comparison as in fig. 9.

The transistor count for CCMOS, TFA, TGA, BBL-PT, ULPFA and SERF are 28T,

16T, 20T, 18T, 24T and 10T respectively which influence the higher power

consumption in their respective circuits than the 13T adder. Another

advantage of the PTL adder is that the design occupies a less chip area. Next

important factor is the speed of operation of all the methods which are being

considered for comparison. To achieve this, the propagation delay should be

smaller to compute the output with respect to the applied input. The delay

taken by the sum circuit to produce a change in the output is smaller for BBL-PT adder than the other methods as in fig. 10(a). The reason is because of the minimum nodes, the signal propagates from its input to output quicker than the rest of the methods. The delay of the carry circuit for the BBL-PT is again less than 13T adder due to the static CMOS used as carry block and hence it is faster as shown in the graph of fig. 10(b). The Power delay products for the sum and carry circuits are hence have the relevant values as given in fig. 11(a) & fig. 11(b) respectively. From the data shown in the table II, the delay is larger for the proposed adder circuit than the other six methods which is applicable for both sum and carry circuit. The reason is the slower mobility of electrons in a pass transistor circuit than the circuit arrangements of the other logic methods taken for comparison. The following few paragraphs give the reason for the increase in the delay of the PTL adder. The average velocity of electron is equal to the product of mobility of charge carriers and electric field which is expressed as, $v = \mu E$ (18) Here, E is the electric field defined as $E = V_{ds}/L$ (19) Where, V_{ds} – Drain –Source Voltage, L – Channel Length of MOS transistors. The drain current is expressed as, $I_{ds} = Q_{channel} v/L$ (20) Where, $Q_{channel}$ – Charge across the channel From equations (18) to (20), it is clear that the velocity of electrons depends on the Electric field which is equal to the drain source voltage [17] – [19]. For the case of 13T, there is signal degradation at the output due to the circuit's dependency on input signal which is not driven by the supply voltage. Hence the potential available in a 13T adder is insufficient to switch the circuit faster like a BBL-PT circuit.

Conclusions

The PTL method of 1 bit full adder cell is implemented in this work along with the CCMOS, TFA TGA, BBL-PT, ULPFA and SERF logic styles to evaluate this type of adder. The objective is met as it is to consume low power which is 33 times less than the BBL-PT adder at the maximum. But the delay of the proposed design is 50% larger than the other methods. This is due to the so called mobility degradation. The other reason is the trade- off between power, delay and area as stated in numerous literatures. The new adder works fine with a minimum PDP in the sum circuit and lack in carry path due to the threshold drop and reduced current driving capabilities. However the PTL adder has the dual advantage of low power and less area. The work may be extended in multipliers to see the scope of its usage in array architectures.