# Piezoelectric energy harvesting power supply engineering essay

Engineering

The LTCR3588-1 integrates a low-loss full-wave bridge rectifier with a high efficiency buck converter to form a complete energy harvesting solution optimized for high output impedance energy sources such as piezoelectric transducers. An ultralow quiescent current under voltage lockout (UVLO) mode with a wide hysteresis window allows charge to accumulate on an input capacitor until the buck converter can efficiently transfer a portion of the stored charge to the output. In regulation, the LTC3588-1 enters a sleep state in which both input and output quiescent currents are minimal. The buck converter turns on and off as needed to maintain regulation. Four output voltages, 1. 8V, 2. 5V, 3. 3V and 3. 6V, are pin selectable with up to 100mA of continuous output current; however, the output capacitor may be sized to service a higher output current burst. An input protective shunt set at 20V enables greater energy storage for a given amount of input capacitance.

## Features of the IC LTC3588-1:

950nA Input Quiescent Current (Output in Regulation – No Load)450nA Input Quiescent Current in UVLO2. 7V to 20V Input Operating RangeIntegrated Low-Loss Full-Wave Bridge RectifierUp to 100mA of Output CurrentSelectable Output Voltages of 1. 8V, 2. 5V, 3. 3V, 3. 6VHigh Efficiency Integrated Hysteretic Buck DC/DCInput Protective Shunt – Up to 25mA Pull-Down at VIN ≥ 20VWide Input Under voltage Lockout (UVLO) RangeAvailable in 10-Lead MSE and 3mm × 3mm DFN packages

## Application of IC LTC3588-1:

Piezoelectric Energy HarvestingElectro-Mechanical Energy HarvestingWireless HVAC SensorsMobile Asset TrackingTire Pressure SensorsBattery Replacement for Industrial SensorsRemote Light SwitchesStandalone Nano-power Buck RegulatorLTC5588-1

## 100mA Piezoelectric Energy Harvesting Power Supply using LTC3588-1

## PIN Configuration OF LTC3588-1:

pincon

## PIN FUNCTIONS:

PZ1 (Pin 1): Input connection for piezoelectric element or other AC source (used in conjunction with PZ2). PZ2 (Pin 2): Input connection for piezoelectric element or other AC source (used in conjunction with PZ1). CAP (Pin 3): Internal rail referenced to VIN to serve as gate drive for buck PMOS switch. A 1µF capacitor should be connected between CAP and VIN. This pin is not intended for use as an external system rail. VIN (Pin 4): Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The VIN voltage is internally clamped to a maximum of 20V (typical). SW (Pin 5): Switch Pin for the Buck Switching Regulator. A 10µH or larger inductor should be connected from SW to VOUT. VOUT (Pin 6): Sense pin used to monitor the output voltage and adjust it through internal feedback. VIN2 (Pin 7): Internal low voltage rail to serve as gate drive for buck NMOS switch. Also serves as a logic high rail for output voltage select bits D0 and D1. A 4. 7µF capacitor should be connected from

VIN2 to GND. This pin is not intended for use as an external system rail. D1 (Pin 8): Output Voltage Select Bit. D1 should be tied high to VIN2 or low to GND to select desired VOUT. D0 (Pin 9): Output Voltage Select Bit. D0 should be tied high to VIN2 or low to GND to select desired VOUT. PGOOD (Pin 10): Power good output is logic high when VOUT is above 92% of the target value. The logic high is referenced to the VOUT rail. GND (Exposed Pad Pin 11): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3588-1.

## ELECTRICAL CHARACTERISTICS:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The LTC3588-1 is tested under pulsed load conditions such that TJ ≈ TA. The LTC3588E-1 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3588I-1 is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (TJ, in °C) is calculated from the ambient temperature (TA, in °C) and power dissipation (PD, in Watts) according to the formula: TJ = TA + (PD • θJA), where θJA (in °C/W) is the package thermal impedance.

Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

## LTC3588-1 Chip Block diagram:

LTC3588-1 chipc block diagram

## Operation of IC LTC3588-1:

The LTC3588-1 is an ultralow quiescent current power supply designed specifically for energy harvesting and/or low current step-down applications. The part is designed to interface directly to a piezoelectric or alternative A/C power source, rectify a voltage waveform and store harvested energy on an external capacitor, bleed off any excess power via an internal shunt regulator, and maintain a regulated output voltage by means of a nano-power high efficiency synchronous buck regulator.

## Internal Bridge Rectifier

The LTC3588-1 has an internal full-wave bridge rectifier accessible via the differential PZ1 and PZ2 inputs that rectifies AC inputs such as those from a piezoelectric element. The rectified output is stored on a capacitor at the VIN pin and can be used as an energy reservoir for the buck converter. The low-loss bridge rectifier has a total drop of about 400mV with typical piezo generated currents (~10µA). The bridge is capable of carrying up to 50mA. One side of the bridge can be operated as a single-ended DC input. PZ1 and PZ2 should never be shorted together when the bridge is in use.

## Under voltage Lockout (UVLO)

When the voltage on VIN rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. A wide (~1V) UVLO hysteresis window is employed with a lower threshold approximately 300mV above the selected regulated output voltage to prevent short cycling during buck power-up. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. Extremely low quiescent current (450nA typical) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

## Internal Rail Generation

Two internal rails, CAP and VIN2, are generated from VIN and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the VIN2 rail serves as logic high for output voltage select bits D0 and D1. The VIN2 rail is regulated at 4. 8V above GND while the CAP rail is regulated at 4. 8V below VIN. These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and VIN2 pins to serve as energy reservoirs for driving the buck switches. When VIN is below 4. 8V, VIN2 is equal to VIN and CAP is held at GND. Figure 1 shows the ideal VIN, VIN2 and CAP relationship. f1

## Buck Operation

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the VOUT sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher

than the regulation point. It does this by ramping the inductor current up to 260mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by VIN, VOUT, and the inductor value. If the input voltage falls below the UVLO falling threshold before the output voltage reaches regulation, the buck converter will shut off and will not be turned on until the input voltage again rises above the UVLO rising threshold. During this time the output voltage will be loaded by less than 100nA. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA of average load current when it is switching. When the sleep comparator signals that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still fl owing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode. The LTC3588-1 keeps the NMOS switch on during this time to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero. Though the quiescent current when

the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy. Four selectable voltages are available by tying the output select bits, D0 and D1, to GND or VIN2. Table 1 shows the four D0/D1 codes and their corresponding output voltages.

## Table 1. Output Voltage Selection

D1D0V outVOUT QUIESCENT CURRENT (IVOUT)0O1. 8v44nA012. 5v62nA1O3. 3v81nA113. 6v89nAThe internal feedback network draws a small amount of current from VOUT as listed in Table 1.

## Power Good Comparator

A power good comparator produces a logic high referenced to VOUT on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed VOUT, signalling that the output is in regulation. The PGOOD pin will remain high until VOUT falls to 92% of the desired regulation voltage. Several sleep cycles may occur during this time. Additionally, if PGOOD is high and VIN falls below the UVLO falling threshold, PGOOD will remain high until VOUT falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost. Figure 2 shows the behaviour for

VOUT = 3. 6V and no load. At t = 75s VIN becomes high impedance and is discharged by the quiescent current of the LTC3588-1 and through servicing VOUT which is discharged by its own leakage current. VIN crosses UVLO falling but PGOOD remains high until VOUT decreases to 92% of the desired regulation point. The PGOOD pin is designed to drive a microprocessor or other chip I/O and is not intended to drive higher current loads such as an LED. f2The D0/D1 inputs can be switched while in regulation as shown in Figure 3. If VOUT is programmed to a voltage with a PGOOD falling threshold above the old VOUT, PGOOD will transition low until the new regulation point is reached. When VOUT is programmed to a lower voltage, PGOOD will remain high through the transition. f3

## Energy Storage

Harvested energy can be stored on the input capacitor or the output capacitor. The wide input range takes advantage of the fact that energy storage on a capacitor is proportional to the square of the capacitor voltage. After the output voltage is brought into regulation any excess energy is stored on the input capacitor and its voltage increases. When a load exists at the output the buck can efficiently transfer energy stored at a high voltage to the regulated output. While energy storage at the input utilizes the high voltage at the input, the load current is limited to what the buck converter can supply. If larger loads need to be serviced the output capacitor can be sized to support a larger current for some duration. For example, a current burst could begin when PGOOD goes high and would continuously deplete the output capacitor until PGOOD went low. The LTC3588-1 harvests ambient vibrational energy through a piezoelectric element in its primary application.

Common piezoelectric elements are PZT (lead zirconate titanate) ceramics, PVDF (poly vinylidene fluoride) polymers, or other composites. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when fl exed as molecules repels each other. Ceramics are often used under direct pressure while a polymer can be fl exed more readily. A wide range of piezoelectric elements are available and produce a variety of open-circuit voltages and short-circuit currents. Typically the open-circuit voltage and short-circuit currents increase with available vibrational energy as shown in Figure 4. Piezoelectric elements can be placed in series or in parallel to achieve desired open circuit voltage. f4The LTC3588-1 is well-suited to a piezoelectric energy harvesting application. The 20V input protective shunt can accommodate a variety of piezoelectric elements. The low quiescent current of the LTC3588-1 enables efficient energy accumulation from piezoelectric elements which can have short circuit currents on the order of tens of micro amps. The LTC3588-1 will gather energy and convert it to a useable output voltage to power microprocessors, wireless sensors, and wireless transmission components. Such a wireless sensor application may require much more peak power than a piezoelectric element can produce. However, the LTC3588-1 accumulates energy over a long period of time to enable efficient use for short power bursts. For continuous operation, these bursts must occur with a low duty cycle such that the total output energy during the burst does not exceed the average source power integrated over an energy accumulation cycle. For

piezoelectric inputs the time between cycles could be minutes, hours, or longer depending on the selected capacitor values and the nature of the vibration source.