Dc power supply design

Abstract: The main aim of this assignment is to design a pre amplifier circuit with an NPN transistor to be used in a simple public address (PA) system. The pre amplifier is fed from a microphone that produces an average output voltage of 10 mV rms. The amplifier is to operate over a frequency range of 300 Hz to 5 kHz and should have an adjustable volume control. The expected gain of the amplifier is 100.

First we are going to design an amplifier for given specifications, model the operation of the circuit using h-parameter and r-parameter model, use computer aided design software to analyze the circuit performance and demonstrate the working of the circuit by hardware implementation. Then, we will plot the frequency response of the circuit and analyze the effect of the emitter bypass capacitor. Finally we will compare the mid-band gain, bandwidth and lower cutoff frequency obtained from the simulation result and the hardware implementation with the designed values. Chapter 1

Introduction: Bipolar Junction Transistor (BJT) is a three terminal device with three regions (Emitter, Base and Collector) and two PN junctions (Emitter-Base junction and Base-Collector junction). Since there are two junctions that means there are four possible ways of biasing a transistor. If both junctions are forward biased then the transistor will operate in the saturation region. If both junctions are reverse biased then the transistor will operate in the cut of region. These two conditions of operation are used when the transistor is needed to work as a switch.

To use a transistor as an amplifier, the emitter base junction should be forward biased and the collector base junction should be reverse biased. Amplifier is an electronic circuit that can amplify signals applied to its input

terminal. If an AC signal is given to a transistor amplifier it will produce an AC base current. This AC base current will produce a much larger AC collector current since IC=? IB. The AC collector current produces an AC voltage across the load resistor RL, thus producing an amplified, but inverted, reproduction of the AC input voltage in the active region of operations.

DC load line is a sloping straight line connecting all the operating points of a transistor biasing drawn on the output characteristics of the transistor and the intersection point gives the Quiescent point (Q-point). A prober Q-point should be in the middle of the DC load line. Selecting a good Q-point prevents the transistor from going into the cutoff or the saturation region and gives more stability. A fixed bias (i. e. base bias) circuit or a voltage divider bias circuit can be used for this assignment but a voltage divider circuit is more efficient.

The main disadvantage in a fixed bias circuit is that ? ac depends on temperature, which means ? ac is not stable. And when ? ac changes, IC will change(IC=? IB) and VCE will change. The changes in IC and VCE make the Q-point unstable. Whereas in voltage divider bias circuit, IC is independent of ? ac and hence the Q-point is more stable. Voltage divider bias is widely used because reasonably good stability reached with a single power supply. Chapter 2 Problem Description: The problem is to design and fabricate a pre amplifier circuit with an NPN transistor to be used in a simple public address (PA) system.

The input of the pre amplifier circuit is taken from a microphone that produces an average output voltage of 10 mV rms. The amplifier is to operate over a frequency range of 300 Hz to 5 kHz. Also, it should have an

adjustable volume control. The expected voltage gain of the amplifier is 100. Design Specifications: Voltage gain = 100 Lower cut off frequency = 300Hz Vin = 10mV (rms) RL = 10k? DC power supply = 10V to 15V Type of transistor – NPN We will begin our assignment by selecting a suitable transistor. Then we will decide on a DC voltage supply and assume a prober Q-point (IC, VCE) to carry out the design.

We will start the design by calculating the values of Resistors RC and RE and the voltage divider resistors R1 and R2. After that we will calculate the values of the two coupling capacitors (C1 and C2) and the emitter bypass capacitor (CE) for the required cut off frequency. After finishing the mathematical model we will simulate the circuit using OrCAD to analyze the circuit performance. Then, after finishing the simulation, we will assemble the circuit using approximate values of the calculated ones. Finally, we will compare the simulation results with the hardware results.

The results we will be focusing on are the voltage gain, the cutoff frequency and the Bandwidth. Chapter 3 Circuit Diagram and Design: Av = 100 FL = 300Hz Av = 100 FL = 300Hz Figure 1 – Circuit Diagram Step1 – Selection of Transistor, Supply Voltage (VCC) and Collector Current (IC): The selected transistor should have a minimum current gain (?) that is equal to or greater than the desired voltage gain. Therefore, we will use Q2N2222 in this assignment. Since the output voltage swing is not specified in this assignment, we will choose 12V as our voltage supply. We will choose IC as 4 mA. Transistor: Q2N2222

Supply Voltage: VCC = 12 V Collector Current: IC = 4 mA * To carry out the design we need to draw the dc equivalent circuit. Figure 2 – DC Equivalent

Circuit Step2 – Design of Collector Resistor (RC) and Emitter Resistor (RE): VCE = 50% VCC = 50% ? 12 = 6 V VE = 10% VCC = 10% ? 12 = 1. 2 V VRC = VCC – VE – VCE = 12 – 6 – 1. 2 = 4. 8 V RC = VRCIC = 4. 8 V4 mA = 1. 2 k? RE = VEIE = VEIC = 1. 2 V4 mA = 300 ? , since IC ? IE Step3 – Design of Voltage Divider R1 and R2: ? = 100 (data sheet) R2 = ? RE10= 100? 30010 = 3 k? VB = VBE + VE = 0. 7 + 1. 2 = 1. 9 V VB = VCCR2R1+R2 R1 = VCCR2VB+R2 = 100? 3k1. +3k = 16 k? * Now we need to draw the ac equivalent circuit. Figure 3 – AC Equivalent Circuit Step4 – Design of RE1 and RE2: RE = RE1 + RE2 Rout = Rc || RL = 1. 2? 101. 2+10= 1 k? r'e = 26mIE = 26mIC = 6. 5 ? AV = Routr'e+RE1 r'e+RE1= RoutAv = 1k100 = 10 ? RE1 = 10 – r'e = 10 – 6. 5 = 3. 5 ? RE2 = RE – RE1 = 300 – 3. 5 = 296. 5 ? Step5 – Design of Coupling Capacitors C1 and C2: hie = Rin (base) = ? (r'e+RE1) = 100 ? (3. 5 + 6. 5) = 1 k? Rin (tot) = R1 || R2 || Rin (base) = 1116+13+11 = 716. 4 ? XC1 = Rin(tot)10 = 716. 410 = 71. 64 ? C1 = 12? fLXC1 = 12?? 300? 71. 64 = 7. 4 µF XC2 = RC + RL = 1. 2 + 10 = 11. k? C2 = 12? fLXC2 = 12?? 300? 11200 = 47. 4 nF Step6 – Design of Bypass Capacitor CE: R’S = R1 || R2 = 16. 09? 316. 09+3 = 2. 5 k? Re = RE2 ||{ R’S ? + (r'e+RE1)} = 296. 5 ||{ 2500 100+ (6. 5+3. 5)} = 296. 5? 35296. 5+35 = 31. 3 ? XCE = Re10 = 31. 310 = 3. 13 ? CE = 12? fLXCE = 12?? 300? 3. 13 = 169. 5 µF Av = 100 FL = 300Hz Av = 100 FL = 300Hz Figure 4 – Circuit Diagram with values Simulation Results: With CE: Mid-band gain, AV = 99. 8 Lower Cutoff Frequency, FL = 334 Hz Higher Cutoff Frequency, FH = 20. 6 MHz Bandwidth, BW = FH – FL = 20. 6 M – 334 = 20. 6 MHz Without CE: Mid-band gain, AV = 3. 5

Lower Cutoff Frequency, FL = 305 Hz Higher Cutoff Frequency, FH = 46 MHz Bandwidth, BW = FH – FL = 46 M – 305 = 46 MHz (Circuit Diagram and Frequency Response are enclosed along with this report) Chapter 4 Hardware Fabrication and Testing Details: During circuit assembling process we tried to find the nearest values to the calculated ones. These are the values we used: RC = 1. 2 k? we selected1. 2 k? RE1 = 3. 5 ? we selected4. 5 ? RE2 = 296. 5 ? we selected270 ? R1 = 16 k? we selected15 k? R2 = 3 k? we selected2. 2 k? C1 = 7. 4 µF we selected10 µF C2 = 47. 4 nF we selected47 nF CE = 169. 5 µF we selected147 µF Procedure: . Assembled the circuit on a breadboard and connected a DC power supply of 12V. 2. Applied a sine wave of 10 mV amplitude and 100 Hz frequency to the input. 3. Observed the output waveform in the CRO and noted down the amplitude. 4. Increased the input signal frequency in steps, without changing its amplitude, and noted down the output amplitude at each step. 5. Calculated the voltage gain of the amplifier by the equation, AV = Vout/Vin found the voltage gain in dB by the equation, AV (dB) = 10 log (AV). 6. Plotted the frequency response curve and found the frequencies (fL and fH) for which the gain reaches 0. 07 of mid band gain. 7. Found the frequency range between fL and fH which gives the bandwidth of the amplifier. Hardware Results: With CE: Frequency (Hz)| Vout (mV)| AV| AV (dB)| log f| 100| 182| 18. 2| 25. 20| 2. 0| 500| 662| 66. 2| 36. 42| 2. 7| 1 k| 750| 75. 0| 37. 50| 3. 0| 5 k| 784| 78. 4| 37. 89| 3. 7| 10 k| 786| 78. 6| 37. 91| 4. 0| 50 k| 786| 78. 6| 37. 91| 4. 7| 100 k| 786| 78. 6| 37. 91| 5. 0| 500 k| 786| 78. 6| 37. 91| 5. 7| 1 M| 786| 78. 6| 37. 91| 6. 0| 2 M| 784| 78. 4| 37. 89| 6. 3| 5 M| 770| 77. 0| 37. 73| 6. 7| 10 M| 728| 72. 8| 37. 24| 7. 0| 50 M| 344| 34. 4| 30. 73| 7. 7| 100 M| 182| 18. 2| 25. 0| 8. 0| Mid-band gain, AV = 78. 6 Lower Cutoff Frequency, FL

= 2. 6 B = 398 Hz Higher Cutoff Frequency, FH = 7. 35 B = 17. 78 MHz Bandwidth, BW = FH – FL = 17. 78 M – 398 = 17. 78 MHz Without CE: Frequency (Hz)| Vout (mV)| AV| AV (dB)| log f| 100| 12| 1. 2| 1. 58| 2. 0| 500| 32| 3. 2| 10. 10| 2. 7| 1 k| 36| 3. 6| 11. 13| 3. 0| 5 k| 38| 3. 8| 11. 60| 3. 7| 10 k| 38| 3. 8| 11. 60| 4. 0| 50 k| 38| 3. 8| 11. 60| 4. 7| 100 k| 38| 3. 8| 11. 60| 5. 0| 500 k| 38| 3. 8| 11. 60| 5. 7| 1 M| 38| 3. 8| 11. 60| 6. 0| 2 M| 38| 3. 8| 11. 60| 6. 3| 5 M| 38| 3. 8| 11. 60| 6. 7| 10 M| 36| 3. 6| 11. 13| 7. 0| 50 M| 26| 2. 6| 8. 0| 7. 7| 100 M| 18| 1. 8| 5. 10| 8. 0| Mid-band gain, AV = 78. 6 Lower Cutoff Frequency, FL = 2. 55 B = 356 Hz Higher Cutoff Frequency, FH = 7. 6 B = 39. 81 MHz Bandwidth, BW = FH – FL = 39. 81 M – 356 = 39. 81 MHz (Frequency responses of the circuit with and without CE are enclosed along with this report) (Frequency responses of the circuit with and without CE are enclosed along with this report) Chapter 5 Discussion and Conclusion: * First of all, there are several ways and various methods to design a common emitter amplifier or so-called RC coupled amplifier that are completely different than the one we used.

We did not choose this method because it is the best method, actually, there is no such a thing called the best method. There are simple ways and there are more accurate ways. It depends on the primary assumptions, the design specifications and the thumb rules used. Simply, the method we used achieved the design requirements and accomplished desired results. * An Amplifier is a circuit that is capable of amplifying signals applied to its input terminal. The main component in any amplifier circuit is usually a transistor.

Since the transistor configuration we used is a common emitter configuration, the circuit is called a Common Emitter Amplifier. Unlike other

configurations, CE amplifier exhibit high voltage gain and high current gain. Generally, the process of a common emitter amplifier can be explained in three steps. First, the AC input signal produces an AC base current. Then, This AC base current will produce a much larger AC collector current since IC=? IB. After that, The AC collector current produces an AC voltage across the load resistor RL, thus producing an amplified, but inverted, reproduction of the AC input voltage. To use a transistor as an amplifier it should be operated in the active region (linear region). To set a transistor in the active region both junctions, Emitter-Base junction and Base-Collector junction, should be forward biased. Since changes in in temperature and other factors during the amplification process may drive the transistor into the cutoff or the saturation region, the Q-point should be in the middle of the active region to enhance the stability of the amplifier. * We preferred using a voltage divider bias circuit over other biasing circuits because in this kind of biasing circuits, IC is independent of ? nd therefore the Q-point is more stable. Voltage divider bias circuit is widely used because of the good stability reached with a single power supply. * C1 and C2 are called coupling capacitors. They pass ac from one side to another and block dc from appearing at the output side. In addition to that, C1 act as a high pass filter on the input signal and its value must be chosen so that it does not attenuate the frequencies which are to be amplified. Similarly, C2 also must be prevented from attenuating the output signal. * The bypass capacitor CE provides an effective short to the ac signal round the emitter resistor RE2, thus keeping only RE1 seen by the ac signal between the emitter and ground. Therefore, with the bypass capacitor, the gain of the amplifier is maximum and equal to AV= Routr'e+RE1 . Without the bypass capacitor,

both RE1 and RE2 are seen by the ac signal between the emitter and ground and effectively add to r'e in the voltage gain formula. Hence, AV= Routr'e+RE1+RE2 . * r'e is a dynamic resistor that depends on temperature. If AV was dependent only on r'e, and RE1 was not there (i. e. AV= Routr'e), AV will be unstable over changes in temperature because when r'e increases, the gain decreases and vice versa.

In order to minimize the effect of r'e without reducing the voltage gain to its minimum value we partially bypassed the total emitter resistance RE. This is known as swamping which is a compromise between having a bypass capacitor across RE and not having a bypass capacitor at all. RE1 should be at least ten times greater than r'e to minimize the effect of it. In our design RE1 is less than r'e and hence it will not do anything other than slightly reducing the gain to be about 100. In other words, in our design RE1 is somehow useless. * At lower frequencies, a capacitor will act as an open circuit.

At higher frequencies, a capacitor will act as a short circuit. That is because the capacitive reactance is inversely proportional to the frequency (XC= 1/2? fC). In an RC coupled amplifier circuits, at lower frequencies, more voltage drops across C1 and C2 because their reactance is very high. This higher signal voltage drop reduces the voltage gain of the amplifier. Similarly, at lower frequencies, the reactance of the bypass capacitor (CE) increases and this reactance in parallel with RE1 create an impedance that reduces the voltage gain.

This is why RC coupled amplifier circuits have less voltage gain at lower frequencies than they have at higher frequencies. However, at higher

frequencies, the reactance of the internal transistor junction capacitance goes down and when it becomes small enough, a portion of the output signal voltage is fed back out of phase with the input, thus effectively reducing the voltage gain. * Our hardware implementation results and simulation results were different. Obviously, that is because we did not find the exact values for our design. There was a notable difference between the design values and the values we have selected, especially for R2.

The cutoff frequency (fL= 398 Hz) is somehow acceptable but the mid band gain (AV= 78. 6) is a little bit less than the desired one. Increasing the value of R2 could have solved the problem. It could have increased the voltage gain and reduced the cutoff frequency. * One of the aims of the design is to have an adjustable volume control. There are several ways to do this. One of them, and I think it’s the best, is by using a variable resistor in place of RE1 (i. e. a 100 ? variable resistor). Basically, this resistor is inversely proportional to the voltage gain (AV= Routr'e+RE1).

Reducing the value of RE1 will increase the voltage gain, thereby increasing the volume and vice versa. References: 1. Theodore F. Bogart, Jefferey S. Beasley and Guilermo Rico (2004). Electronic Devices and Circuits. India: Pearson Education, Inc. 2. Thomas L. Floyd (2005). Electronic Devices. 7th ed. India: Pearson Education, Inc. 3. HyperPhysics (2004) Common Emitter Amplifier,[online] Available at: http://hyperphysics. phy-astr. gsu. edu/hbase/electronic/npnce. html [Accessed: 20th Nov 2011]. 4. Scribd (2006) Common Emitter Amplifier, [online] Available at: http://www. cribd. com/doc/27767944/Common-Emitter-Amplifier [Accessed: 25th Nov 2011]. 5. Visionics (2005) RC Coupled Amplifier, [online] Available at:

http://www. visionics. ee/curriculum/Experiments/RC%20Ampr/RC%20Coupled%20Amplifier1. html [Accessed: 1st Nov 2011]. 6. SSIT (2006) Analog Electronic Circuits, [online] Available at: http://www. ssit. edu. in/dept/assignment/aeclabmanual. pdf [Accessed: 5th Nov 2011]. 7. Edutalks (2007) RC Coupled Amplifier, [online] Available at: http://www. edutalks. org/electronics%20lab%20manual%201. pdf [Accessed: 7th Nov 2011].