Silicon waveguide fabrication processes engineering

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- Decision

Today, it is known that high informations rate communicating requires the replacing of conventional Cu engineering with optical engineering. Photonic circuits is a important technological invention that forms the nucleus of the optical communicating system which reduces infinite and power ingestion, and improves dependability. Silicon is the cardinal campaigner which provides good public presentation in photonic circuits at low cost. Silicon photonics promises a low cost optical devices and really high velocity informations bringing.

The important edifice block of every photonic circuit is the optical wave guide. The first Si wave guides were presented in the 1980s, in Si on doped Si, Si on sapphire, silicon Ge and Si on dielectric (SOI) [1] . Among these wave guides silicon on dielectric is the most popular one.

Silicon as a photonic medium has major advantages. Due to the copiousness and low cost of Si, industries are able to bring forth microprocessors with 1000000s of transistors in it and offer them at a really low monetary value. Silicon has a higher thermic conduction when compared to III-V compounds. Furthermore, Si on dielectric (SOI) provides an ideal platform for making two-dimensional waveguide circuits. The refractile index contrast between Si (n= 3. 45) and SiO2 (n= 1. 45) , allows tight optical parturiency and makes it possible to scale photonics devices to the submicron dimensions [2] .

The high refractile index difference between Si and SiO2 is besides a disadvantage. This causes the transmittal dispersing loss from interface

imperfectnesss associated with fiction procedures [3] . For Si wave guides, the sidewall raggedness is the major cause for the transmittal loss and this sidewall raggedness additions with the addition in the refractile index difference between the nucleus and cladding interface. The light extension losingss strongly increase with the refractile index difference and the sprinkling from the raggedness becomes major beginning of light transmittal loss, which scales with the square of the raggedness amplitude [3] .

The wave guide sidewall raggedness can be reduced by a technique called smoothing. Many smoothing techniques have been proposed and they were successful in cut downing the sidewall raggedness such as tempering, oxidization and wet chemical etching and so on.

1. 2 Aim

In this experiment extension losingss of silicon wave guides of different breadths runing from 500nm to 900nm are measured. This sample is so cleaved in to two pieces and made to undergo through the procedure of oxidization and the extension losingss are measured once more. At last, this sample undergoes through the procedure of tempering and the losingss are measured. A comparing is made between these three losingss.

1. 3 Outline

Chapter 2 nowadayss an overview of Silicon photonics and its applications in different Fieldss.

Chapter 3 gives an overall thought of Silicon waveguide fiction procedure.

Chapter 4 describes the extension losingss in Si wave guide and its causes.

Chapter 5 describes different smoothing techniques used for the decrease of sidewall raggedness of Si wave guides

Chapter 6 explains the theoretical portion of silicon waveguide loss measurings and besides gives the experimental consequences. This chapter besides explains the Fabry-Perot interferometric method.

Chapter 7 presents the decision.

Chapter 2

Silicon Photonics

Photonics is the scientific discipline and engineering of visible radiation and Si photonics is the survey and application of photonic system which uses Si as an optical medium [4] . As the engineering advanced, the interconnects within the micro chip go a large job and optical interconnects are seen as promising manner frontward. The silicon photonics became possible when photonics maps were integrated in to the engineering. Silicon photonics integrates both negatron and optical constituent on the same Si bit [4] . These operates in the infrared part, largely at 1500nm wavelength used by most fibre ocular telecommunication system [5] .

The ground for taking the Si as a nucleus stuff in the photonics industries is because of the many advantages of Si. Silicon is widely available stuff and Si wafers have the lowest monetary value and good crystal quality compared to any other semiconducting material stuff. Silicon signifiers into silicon di-oxide when it reacts with the O. This oxide bed can be used as an dielectric. Another ground is the handiness of Si on dielectric, an ideal platform for

making two-dimensional wave guide. The big refractile index contrast between Si (n = 3. 45) and SiO2 (n = 1. 45) makes it possible to scale photonic devices to a really little graduated table (100s of nanometer) [2] .

2. 1 Silicon on Insulator (SOI) substrate

SOI substrates are an of import component in the Si photonics engineering. The visible radiation is confined to the nucleus (Si) by the top and bottom facings (silicon dioxide) . The high refractile index contrast between the nucleus and the facing does non let the visible radiation to widen into the cladding part. The rib construction on top of the device guides the visible radiation in the plane of the Si. The illustration is shown in the figure.

There are two types to manufacture SOI substrate. They are SIMOX procedure and wafer bonding.

SIMOX – In this method O is implanted into Si wafer into certain deepness and so bring on an oxidization procedure inside the Si wafer by tempering [6] .

Wafer adhering – Here two wafers are coated with the oxide bed and so both Si wafers are pressed against each other at a high temperature making one individual wafer.

2. 2 Applications

Optical Modulation – For a higher transition speed the design of the conventional optical modulator has to be changed. This is done by replacing

the lossy polycrystalline rib with crystalline Si leting the on bit extension loss of the full modulator to be controlled to 10 dubniums [7] .

Optical Interconnects – With the advancement in the computing machine engineering, it is going more dependent on the high velocity informations transportation between the micro chips. Here optical interconnects can be used to supply high velocity informations transportation.

Silicon photonics can be used as an optical router and signal processor for optical communicating.

Silicon photonics can increase the internet velocity by increasing the bandwidth by supplying the micro-scale, extremist low power devices. A paradigm 80km, 12. 5Gbits/s transmittal has late been reported utilizing microring silicon device [8]

Chapter 3

Silicon Waveguide Fabrication Processes

3. 1 Introduction

Semiconductor fiction is the procedure of fabricating IC ' s that are used in electronic devices. The term wafer refers to the handbill phonograph record which is the basal stuff in semiconducting material fiction. Semiconductor device fiction includes multiple stairss during which electronic circuits are bit by bit created on a wafer. Silicon is about ever used. The basic process or procedure in the semiconducting material fiction engineering involves a figure of stairss [9] :

Wafer Growth: Creation of single-crystal substrate stuff.

Lithography: This is the procedure for specifying the form by using thin unvarying bed of photoresist on the wafer surface. The photo-resist is hardened by baking and selectively removed by projection of visible radiation through a photomask incorporating mask information.

Etching: This is the procedure of taking the unwanted stuffs selectively from the surface of the wafer.

Deposition: Movies of the assorted stuffs are applied on the wafer. There are two types of procedures are available for this, they are: physical vapor deposition (PVD) and chemical vapor deposition (CVD) .

Chemical Mechanical Polishing: A planarization technique by using a chemical slurry with etchant agents to the wafer surface.

Oxidation: In the oxidization procedure O (dry oxidization) or H2O (wet oxidization) molecules convert Si beds on top of the wafer to silicon dioxide.

Ion Implantation: This technique is used to present dopant drosss into semiconducting material. The ionised atoms are accelerated through an electrical field and targeted at the semiconducting material wafer.

Diffusion: A diffusion measure following ion nidation is used to temper bombardment-induced lattice defects.

3. 2 SOI based wave guide fiction

The SOI wafer consists of three beds. A top bed of Si which is patterned and becomes the steering nucleus of the wave guide. Below the nucleus bed is

the Buried Oxide bed which forms the lower facing of the wave guide. The bottom bed is the majority Si which gives the stableness to the wafer.

The procedures which are used to manufacture wave guide on SOI substrate are described below:

The first measure is the substrate readying. It is done for bettering the photoresist stuff adhesion to the substrate. Otherwise, any sort of atom attached to the Si surface increases the spread between the mask and the sample. This consequences in uneven deployment of forms ensuing in the raggedness. Substrate readying can be done by one or more procedures like-substrate cleansing for taking the taint, desiccation bake for taking the H2O, and add-on of an adhesion booster [9] .

An oxide bed is grown on top of the substrate (Fig. 3) and so photoresist is applied to the Centre of the oxidized SOI wafer. The wafer is so accelerated quickly to a rotational speed in the scope 3000 to 7000 revolutions per minute for some 30 to 60 seconds [9] . This action spreads the solution uniformly on the wafer (Fig 4) . The intent of the oxide bed beneath the photoresist is to guarantee the protection of the wave guide top surface during Si etching [10] .

After surfacing, the ensuing resist will incorporate between 20 – 40 % dissolvers. The prebake procedure involves drying the photoresist after the spin coat by taking the extra dissolver. The following measure is the alliance and exposure. Here the form of the photomask, which includes the wave guide construction, is transferred to the wafer utilizing photolithography [10] . Exposure is done utilizing the mask aligner. This tool brings resist

covered wafer close to the photomask. After alliance, the wafer is exposed to the visible radiation through photomask, which forms the form on the resist [10] . This is shown in the below figure.

The following procedure is called Development. It uses a chemical that removes the unwanted photoresist, go forthing behind the printed form on the mask depending on whether it is a positive or negative photoresist (Fig. 6) . This measure is followed by the oxide etching for taking the unwanted oxide bed. This can achieved by either reactive ion etching (RIE) or hydrofluoric (HF) solution. This is shown in figure 7.

The following measure is silicon etching. Here a suited procedure must be selected to etch really deep constructions with about perpendicular sidewalls. It is recommended that, about 90 deg verticalness and low etching harm are really of import demand for waveguide fiction (Fig. 8) [10] . This is followed by the remotion of the resist (Fig. 9) and eventually the wafer is masked by the oxide bed which acts as the upper facing bed (Fig. 10) . After these stairss the wave guide construction is complete.

Chapter 4

Propagation losingss in Silicon wave guides

While the electronic devices are widely fabricated on the Si platform, Si photonics devices are still under geographic expedition because of the deficiency of efficient extension of light [11] . These extension losingss are chiefly because of the sidewall raggedness. The fiction measure which causes sidewall raggedness are: sample readying, photoresist spinning, exposure, hardbake and etching. The extension losingss addition as the

wave guide dimensions shrinks [11] . In order to acquire the effectual transmittal, the extension losingss throughout the wave guide must be reduced. In this chapter, we will discourse about the extension losingss in wave guides and the techniques to command them.

Waveguides with the size of few nanometers are imperative for its possible usage in micro chips as an optical interconnector and its usage in incorporate optics. A survey has been done to happen the relationship between the transmittal loss of silicon wave guide and its breadth. This survey accurately predicts that the loss increases as the wave guide breadth decreases [12] . Furthermore, the sidewall raggedness is the major beginning of loss. The figure. 11 shows sidewall raggedness in Si wave guide [14]

The high index difference (a?†n) between nucleus and cladding offers size advantage i. e. the device size graduated tables down with the increasing a?†n. This helps us to incorporate 1000000s of optical devices on a little bit. Conventional treating engineering of Si integrated circuit can be employed since Si and SiO_2 are used as nucleus and cladding stuff. High packing denseness and mass production leads to high output and low cost.

Here, we conduct an experiment to happen the consequence of decrease in the waveguide dimensions on transmittal loss. The figure. 12 shows the transmittal loss observed for the different wave guide with the different breadths [12] . From the figure we can see that the loss is undistinguished for waveguide breadth above 4µm, bespeaking negligible losingss from core-cladding interface and from soaking up. But as the breadth is reduced below

4μm, the loss gets increases. This means in the loss is attributed to the sidewall raggedness which is created during the procedure of photolithography and reactive ion etching [12] .

The sidewall raggedness, sometimes referred as line border raggedness is represented by a one dimensional distribution with zero-mean called degree Fahrenheit (omega) [13] . As shown in the Fig. 13, degree Fahrenheit (omega) is the divergence of the existent border from the idealised heterosexual border. The nature of the raggedness is described by the autocorrelation map of degree Fahrenheit (omega) given by [13] ,

R (u) = { degree Fahrenheit (omega) degree Fahrenheit (z+u) }

An analytical attack can be made to obtain the relationship between the scattering loss and the sidewall raggedness. This is possible by Payne and Lacey attack, which relates the soaking up coefficient to the standard divergence (?) and the autocorrelation length (Lc) [12] . ? can be obtained from mensurating the divergence of degree Fahrenheit (omega) from idealized consecutive line and Lc can be measured from autocorrelation map. The fading coefficient (?) can be expressed as [12]

Where K is free infinite moving ridge vector, vitamin D is the waveguide half-breadth, n1 is the refractile index of the nucleus, g and iron are maps of parametric quantities defined by Payne and Lacey [12] . Above look shows that the loss increases with the average square divergence of surface raggedness (?) and as the waveguide dimension is reduced the scattering loss additions quickly.

Chapter 5

Smoothing Technique

We have already discussed that, how the sidewall raggedness additions as the addition in the core-cladding refractile index difference (a?†n) . The relation between the sidewall raggedness and the sprinkling loss has explained by Lee et al. [16] . Many experiments have been done to get the better of the job of sidewall raggedness to cut down the sprinkling loss.

5. 1 Oxidation:

This procedure is done to take any dangling bonds and the trap charges from either reactive ion etching or electron beam lithography [15] . This procedure is done in an oxidization oven at a really high temperature utilizing O2 gas. This paper presents two types of oxidization procedures [16] . The first procedure of oxidization is done at a changeless temperature (1000 & A ; deg ; C) for different clip and the 2nd procedure is done to demo the dependance of the raggedness on the oxidization temperature [16] .

The Fig. 14 shows the sidewall of the sample oxidized at 1000 & A ; deg ; C: (a) without oxidization (B) for the oxidization clip of 18 min, (degree Celsius) for 75 min and (vitamin D) 165 min. From the Fig. 14 we can see that, as the oxidization clip additions, the raggedness decreases. Fig. 15 shows the oxidization of sample at 900 & A ; deg ; C for 877 min, at 1000 & A ; deg ; C for 175 min and at 1100 & A ; deg ; C for 50 min [16] . We can see that as the temperature is increased, there is a important advancement in the raggedness smoothing. The difference between the two procedure is that the

oxide thickness remain changeless in the 2nd procedure whereas, the oxide thickness additions with the addition in the clip in the first procedure.

5. 2 Annealing:

In this procedure the sample is annealed by utilizing H at assorted force per unit area (runing from 10 to 760 Torr) and at assorted temperature (runing from 900 to 1100 & A ; deg ; C) for approximately 3 to 10 proceedingss [17] . It is been observed that the sidewall raggedness decreases to a great extent by the procedure of H tempering.

5. 3 Wet Chemical Oxidation:

There are tonss of surveies which shows that the oxidization of unsmooth Si for smoothing has been successful. But in footings of stuff ingestion to roughness amplitude decrease, this technique has been proved as an uneffective attack [18] . Hence an alternate oxidization method is employed and it is called ‘ wet chemical oxidization ‘ [19] .

In wet chemical oxidization, Si wave guide after fiction is subjected to one of the four formulas [19] as shown in the table1.

Recipe

Stairss

Repeats

5 x RCA

10 min SC1, DI rinse, 15 s HF,

5

DI rinse, 15 min SC2, DI rinse.

5 x RCA

10 min SC1, DI rinse, 15 s HF,

5

DI rinse.

Extended SC1

50 min SC1, DI rinse, 30 s HF,

1

DI rinse.

5 x Piranha

5 min Piranha, DI rinse, 30 s HF

5

DI rinse

Table 1: Wet chemical oxidization formula.

Here DI rinse is the deionised H2O, SC1 solution consists of DI H2O, H2O2, NH4 OH in 5: 1: 1 ratio, which is used to take organics and to clean surface drosss [19] . The oxides which is formed during SC1 is removed by the

diluted hydrofluoric acid (HF) . SC2 is used to take residuary metals from the surface.

After the RCA intervention, surface raggedness is measured utilizing atomic force microscope (AFM) . Roughness amplitude (?) and the correlativity length (Lc) are obtained as we discussed in the old chapter.

5. 4 Sidewall smoothing by KrF Excimer Laser Reformation:

The dry oxidization and tempering procedure are done at really high temperature. Therefore they have a thermic budget restraints and the procedure of dry oxidization and wet chemical oxidization have low capacity of cut downing big raggedness.

To get the better of these jobs, an alternate method known as KrF excimer optical maser reformation can be used for sidewall smoothing [20] . This method has no thermic budget restriction and can cut down the sidewall raggedness to a great extent.

In this procedure a really high energy KrF excimer optical maser pulsation with a wavelength of 248nm and energy denseness up to 2J/cm? is used to run the sidewall of the Si wave guide [20] . This liquefied Si of sidewall reforms because of the surface tenseness and the ridge profile besides changes [20] . This procedure is capable of cut downing the sidewall raggedness from 14 to 0. 24nm [20] .

Chapter 6

Propagation Loss Measurement

In photonic circuit it is of import to mensurate the extension losingss in wave guides to guarantee its suitableness for the specific application. Since the size of the optical wave guide is really little when compared to optical fiber, it becomes really hard to mensurate the transmittal loss accurately. Many techniques have been proposed for the effectual measuring of the extension losingss such as prism matching method, cut back method, scattered light measuring method, Fabry-Perot interferometric method and so on [21] . The restriction of the prism matching method is that it is limited by the quality of the wafer surface [22] . In cutback method, it becomes really hard to hold the same yoke efficiency for different lengths over multiple measurings [22] .

In this paper we will discourse a technique called Fabry-Perot interferometric method for the waveguide loss measuring. This method is advantageous for low loss wave guides, since it is based on the measuring of the contrast of a Fabry-Perot pit consisting of an optical wave guide with the contemplation from end aspects [21] . For this method the cognition of input yoke is non required.

6. 1 Basic description of FP interferometer:

This consists of a brace of partly brooding, somewhat wedged optical flats placed at a certain distance apart, with the reflecting surface confronting each other [23] . Here, visible radiation is emitted from a beginning set at a focal plane. The light beam is multiple reflected within the mated flats and

produces multiple familial beams. These beams are collected by the focussing lens. The complete intervention form takes the form of a homocentric rings [23] . This is shown in the Fig. 16

6. 2 Loss Measurement theory:

The terminal aspect of SOI wave guide is similar to the Fabry-Perot pit of a optical maser and this is shown in the figure17. If the incident visible radiation is normal to the aspects, the transmittal strength from the FP pit is given by [22] :

Where G is the fading coefficient and ? is the unit of ammunition trip stage displacement. R is the mirror coefficient of reflection, which is calculated from the effectual index measuring of the air and wave guide as

L is the entire pit length and this can be measured from the free spectral scope (FSR) of the Fabry-Perot resonance periphery [24] . Where a?†? is the free spectral scope of the spectral resonance periphery and it is shown in the Fig. 18. L is given by

The extension loss can be determined utilizing the undermentioned expression:

Where R is the ratio between the upper limit and the lower limit of the transmittal strength.

6. 3 Experiment set up:

The experimental set up for the loss measuring of the sample is shown in the Fig. 19. In this peculiar experiment, wave guide of different breadth (runing

from 500nm to 900nm) were characterized in a so called ‘ end-fire ‘ yoke technique. This technique does non necessitate any excess yoke parts and simple cleaving is adequate. Although, attention must be taken to aline the sample by ever keeping the maximal end product power at a fixed wavelength.

This technique includes a optical maser beginning, a chopper, a TE filter, lock-in-amplifier, photodetector, camera and a computing machine which controls the optical maser beginning through lock-in-amplifier via GPIB port. Here a optical maser beam of wavelength 1520nm and with a power of 3mW is emitted from the optical maser beginning. This beam is TE filtered and modulated by a chopper at a frequence of 320 Hz. These modulated beam is made to go through through the Si wave guide which is placed in between the brace of 40x lenses. The camera can be used for the alliance and a Ge photodiode is used for the sensing. The peripheries are observed utilizing a package, TUNICS_TODD V2. 2. vi.

6. 4 Experimental Consequences:

The Fig. 20 shows the Fabry-Perot peripheries obtained for a wave guide with breadth of 900nm. Here, foremost the free spectral scope is calculated and so the pit length calculated, which was found to be 8mm. ‘ r ‘ is calculated by happening the ratio between the upper limit and lower limit of the transmittal strength. The effectual refractile index of Si is considered as 3. 5 and utilizing this mirror coefficient of reflection R is calculated (R= 0. 3) . Using all these values propagation loss is calculated utilizing the expression, which was discussed before. A series of measuring is done like this for a

waveguide breadth runing from 500nm to 900nm to happen the extension loss. These losingss are shown in the Fig. 21.

The oxidization was conducted at 950 & A ; deg ; C for 5 proceedingss with a thickness of 10nm. Annealing was performed at 380 & A ; deg ; C for 15 proceedingss. Propagation losingss were calculated for the same Si wave guide after the procedure of oxidization and tempering and is shown in the Fig. 22 and Fig. 23 severally.

Chapter 7

Decision

A Si wave guide sample with its breadth runing from 500nm to 900nm was used for the extension loss measuring. This study demonstrates how the fiction procedure causes sidewall raggedness and the techniques used to cut down the sidewall raggedness. This study besides shows the ‘ end-fire ‘ yoke technique which is used for the extension loss measuring.

From the experiment we have noticed that the extension loss additions with the lessening in the breadth of the wave guide. This study shows the addition in the extension loss after the oxidization of the sample and a little lessening in the extension loss after the procedure of tempering.